

# To Optimize or Not To Optimize: **Algorithm Design in VLSI CAD**

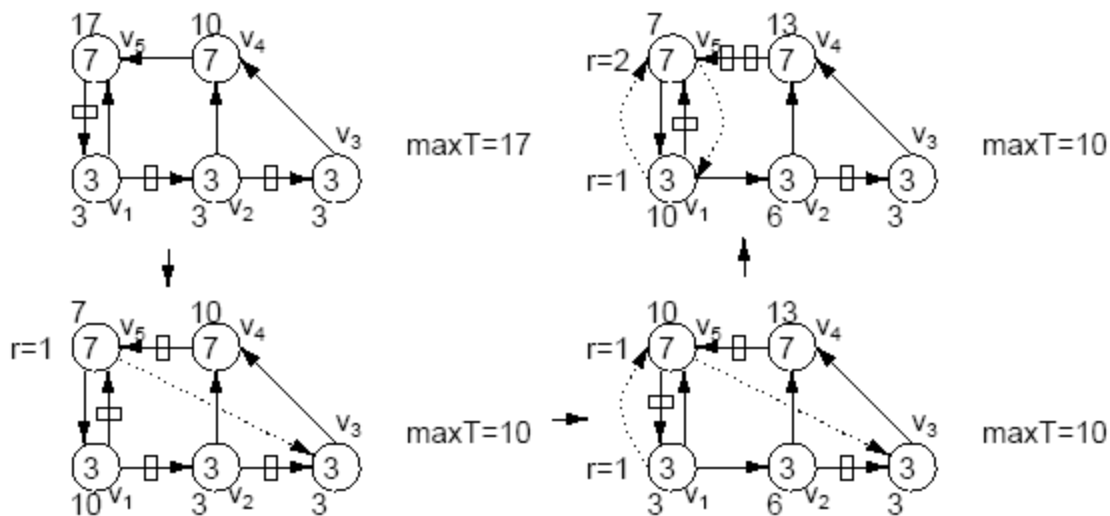
Speaker: Dr. Hai Zhou

## **SEMINAR: MEET THE EECS FACULTY** **Ford Design Center, ITW Auditorium**

(Go to Tech 2<sup>nd</sup> floor, take bridge south to Ford, go down one floor.

From Ford main entrance, go up one floor)

**2:00 -3:00pm, Tuesday May 16, 2006**



As in other engineering disciplines, many problems in VLSI CAD are optimization problems. How to effectively solve them is a question of both practical importance and intellectual depth. What is the difference between optimization problems and non-optimization problems? Shall we optimize or not optimize? In this talk, I will discuss a couple of VLSI CAD problems and their algorithm design. The problems include logic gate sizing for noise control and circuit retiming for clock period minimization. They are important in CAD and the algorithms we designed are provably optimal and efficient. On the other hand, they can be viewed as case studies for algorithm design methodologies. I will also share the joy and lessons I learned from them.

Hai Zhou is an assistant professor in Electrical Engineering and Computer Science at Northwestern University. He got his Ph.D. degree in Computer Sciences from the University of Texas at Austin in 1999. Before joining the faculty of Northwestern University, he was with the Advanced Technology Group at Synopsys, Inc. His research interests include VLSI computer-aided design, algorithm design, and formal methods. He is a senior member of IEEE and a recipient of a CAREER Award from the National Science Foundation in 2003.

ALSO:

Tues May 30: EECS Professor Kristian Hammond:

“Theory and Practice of Needles and Haystacks: Stories from the InfoLab”

Interested in giving a talk next fall?

Contact Jack Tumblin [jet@cs.northwestern.edu](mailto:jet@cs.northwestern.edu) or Thrastos Pappas [pappas@ece.northwestern.edu](mailto:pappas@ece.northwestern.edu)