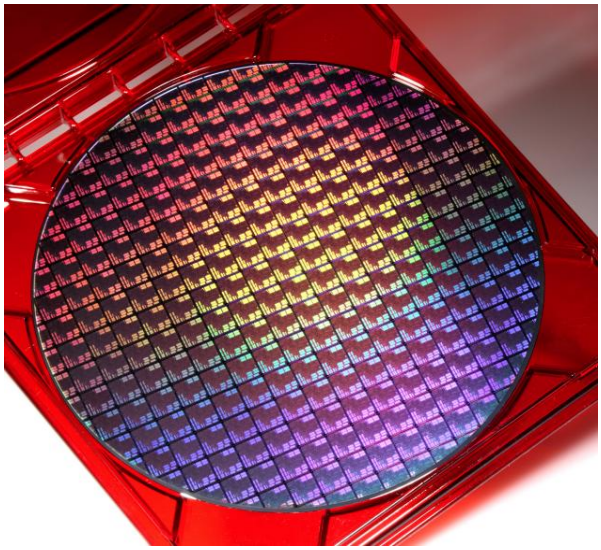
EECS 361 Homework 1
Fall 2006
Due: 10/05/06

1. [10] What is the approximate cost of a die in the wafer shown in Figure 1? Assume that an 8-inch wafer costs $1000 and that the defect density is 1 per square centimeter. Use the number of dies per wafer given in the figure caption.

Some Necessary Equations:

$$\text{Cost per die} = \frac{\text{Cost per wafer}}{\text{Dies per wafer} * \text{yield}}$$

$$\textit{Yield} = \frac{1}{\left(1 + \frac{\text{Defects per area} * \text{Die area}}{2}\right)^2}$$



(Fig 1) An 8 inch (200-mm) diameter wafer containing Intel Pentium processors. The number of Pentium dies per wafer at 100% yield is 196. The die area is 91 mm^2, and it contains about 3.3 million transistors.

2. [5] DRAM chips have significantly increased in die size with each generation, yet yields have stayed about the same (43% to 48%). Figure 2 shows key statistics for DRAM production over the years.

Given the increase in die area of DRAMs, what parameter (see the equations) must improve to maintain yield?

(Fig 2)

Year	Capacity (Kbits)	Die area (sq. cm)	Wafer diameter (inches)	Yield
1980	64	0.16	5	48%
1983	256	0.24	5	46%
1985	1024	0.42	6	45%
1989	4096	0.65	6	43%
1992	16384	0.97	8	48%

3. [5] Consider two different implementations, M1 and M2, of the same instruction set. There are four classes of instructions (A, B, C, and D) in the instruction set.

   M1 has a clock rate of 500 MHz. The average number of cycles for each instruction class on M1 is as follows:

Class	CPI for this class
A	1
B	2
C	3
D	4

   M2 has a clock rate of 750 MHz. The average number of cycles for each instruction class on M2 is as follows:

Class	CPI for this class
A	2
B	2
C	4
D	4

   Assume that peak performance is defined as the fastest rate that a machine can execute an instruction sequence chosen to maximize that rate. What are the peak performances of M1 and M2 expressed as instructions per second?

4. [10] If the number of instructions executed in a certain program is divided equally among the classes of instructions in Problem 3, how much faster is M2 than M1?

5. [5] Assuming the CPI values from Problem 3 and the instruction distribution from Problem 4, at what clock rate would M1 have the same performance as the 750-MHz version of M2?

6. [5] The table below shows the number of floating-point operations executed in two different programs and the runtime for those programs on three different machines:

Program	Floating-point operations	Execution time in Seconds		
		Computer A	Computer B	Computer C
Program 1	10,000,000	1	10	20
Program 2	100,000,000	1000	100	20

Which machine is fastest according to total execution time? How many times faster is it than each of the other two machines?

7. [15] Suppose we have made the following measurements of average CPI for instructions:

Instruction	Average CPI
Arithmetic	1.0 clock cycles
Data transfer	1.4 clock cycles
Conditional branch	1.7 clock cycles
Jump	1.2 clock cycles

Compute the effective CPI for MIPS. Average the instruction frequencies for gcc and spice in Figure 3 to obtain the instruction mix.

(Figure 3) MIPS instruction classes, examples, correspondence to high-level program language constructs, and percentage of MIPS instructions executed by category for two programs, gcc and spice.

Instruction class	MIPS examples	HLL correspondence	Frequency	
			gcc	Spice
Arithmetic	`add, sub, addi`	Operations in assignment statements	48%	50%
Data transfer	`lw, sw, lb, sb, lui`	References to data structure, such as arrays	33%	41%
Conditional branch	`beq, bne, slt, slti`	if statements and loops	17%	8%
Jump	`j, jr, jal`	Procedure calls, returns, and case/switch statements	2%	1%