Abhishek Das

Northwestern University
Dept. of EECS
2145 Sheridan Road
Evanston, IL 60208

Cell: (847) 757-2716
Office: (847) 467-4610
http://www.eecs.northwestern.edu/~ada829
a-das@northwestern.edu

Research Interests

My research interests range from system level microarchitecture to application specific high performance architectures. Most of my research projects involve simulation-based modeling and evaluation. Some of the recent topics include:

- Novel cache and directory management techniques for optimizing power and performance in large scale chip multiprocessors [Under Submission]
- Micro-architectural techniques for efficient speed binning and optimization of chip yield/revenue [DAC'10, MICRO'08, CAL'07, ASGI'07]
- Detection of Hardware Trojan on memory bus using binary instrumentation [DATE'10]
- Reconfigurable Architectures for Network Intrusion Detection System [TIFS'08, DATE'08]
- Power-aware voltage assignment in multicore processors [ICCD'07]

Education

Ph.D. in Computer Engineering, Sept. 2005 – Aug. 2010 (expected)

NORTHWESTERN UNIVERSITY, Evanston, IL USA.
Department of Electrical Engineering and Computer Science
Advisors: Prof. Alok Choudhary and Prof. Gokhan Memik
Current GPA: 3.9/4.0

B.Tech. in Computer Science & Engineering, June 2001 – May 2005

INDIAN INSTITUTE OF TECHNOLOGY, Kharagpur, India.
Department of Computer Science and Engineering
Graduated with GPA: 8.1/10

Publications

[DAC'10] *Quantifying and Coping with Parametric Variations in 3D-Stacked Microarchitectures.*
S. Ozdemir, P. Yan, **A. Das**, G. Loh, G. Memik, and A. Choudhary**.**
Design Automation Conference (DAC), Anaheim, CA, June 2010.

[DATE'10] *Detecting/Preventing Information Leakage on the Memory Bus due to Malicious Hardware.*
A. Das, S. Misra, S. Joshi, J. Zambreno, G. Memik and A. Choudhary.
Design, Automation & Test in Europe (DATE), Dresden / Germany, March 2010.

[TIFS'08] *An FPGA-based Network Intrusion Detection Architecture.*
A. Das, D. Nguyen, J. Zambreno, G. Memik, and A. Choudhary.
IEEE Transactions on Information Forensics and Security (TIFS), Volume 3, Issue 1, March 2008 Pages: 118-132.

[MICRO'08] *Evaluating the Effects of Cache Redundancy on Profit.*
A. Das, B. Ozisikyilmaz, S. Ozdemir, G. Memik, J. Zambreno and A. Choudhary.
International Symposium on Microarchitecture (MICRO-41), Lake Como / Italy, Nov. 2008.

[DATE'08] *An Efficient FPGA Implementation of Principal Component Analysis based Network Intrusion Detection System.*
A. Das, S. Misra, S. Joshi, J. Zambreno, G. Memik and A. Choudhary.
Design, Automation & Test in Europe (DATE), Munich / Germany, March 2008.

[ICCD'07] *Evaluating Voltage Islands in CMPs under Process Variations.*
A. Das, S. Ozdemir, G. Memik and A. Choudhary.

International Conference of Computer Design (ICCD), Lake Tahoe, NV, October 2007

[CAL'07] *Microarchitectures for Managing Chip Revenues under Process Variations.*
A. Das, S. Ozdemir, G. Memik, J. Zambreno, and A. Choudhary.
IEEE Computer Architecture Letters (CAL), Volume 6, June 2007.

[ASGI'07] *Mitigating the Effects of Process Variations: Architectural Approaches for Improving Batch Performance.*
A. Das, S. Ozdemir, G. Memik, J. Zambreno, and A. Choudhary.
Workshop on Architectural Support for Gigascale Integration (ASGI), San Diego, CA, June 2007.

[FCCM'06] *A Reconfigurable Architecture for Network Intrusion Detection Using Principal Component Analysis.*
D. Nguyen, **A. Das**, G. Memik, and A. Choudhary.
IEEE Field-Programmable Custom Computing Machines (FCCM), Napa, CA, April 2006. (Poster)

Work Experience

Graduate Research Assistant
09/2005 – present

Northwestern University, Evanston, IL
Department of Electrical Engineering and Computer Science
Member of Center for Ultra-scale Computing and Information Security (CUCIS)
Director: Prof. Alok Choudhary, and,
Micro-architecture Research Lab **Director: Prof. Gokhan Memik**

Graduate Intern
06/2008 – 08/2008

Intel Corporation, Hillsboro, OR.
Designed and implemented a software architecture that uses zero knowledge authentication for secure key exchange in Intel platforms. The project was in collaboration with Software Solutions Group and Corporate Technology Group within Intel. **Manager:** David Riss

Graduate Intern
06/2007 – 09/2007

Intel Corporation, Hillsboro, OR.
Designed and implemented a Trust Establishment protocol for securing Intel business platforms (vPro). The work involved development of a software prototype which was tested on Intel hardware. **Manager:** David Riss

Teaching Experience

Teaching Assistant, Department of Electrical Engineering and Computer Science
Course: Graduate Computer Architecture — Fall, 2006 and 2007
(Overall Course Rating 5/6)

Software Development

NUCA cache simulator: Cache management modules for a full system multiprocessor simulator (simflex) for non-uniform cache architectures. (C++/Python)

Process Variation Simulator: Automated HSPICE net-list generator for Cache Critical Path based on CACTI
Fine-grain device parameter mapping under process variation (C++/Perl)

Trust Establishment Protocol: C++ prototype (~6000 lines) for a secure communication protocol between Intel platforms. (Released internally at Intel Corp.)

Awards and Honors

May 2001 Among the top 0.1 percent in IIT Joint Entrance Examination in India (200,000 participants).

1999-2001 Merit certificate holder under National Scholarship Scheme for being among the top 100 in board examinations (10th and 12th grades).

Dec. 2000 Ranked 12th in the state of West Bengal (India) in Association for Improvement of Mathematics Teaching (AIMT) competence test, 2000.

Professional Service

External Reviewer IEEE/ACM International Symposium on Microarchitecture (MICRO), IEEE Design Automation & Test in Europe (DATE), IEEE Transactions on Information Forensics and Security, IEEE Journal of Low Power Electronics (JOLPE), ACM Great Lakes Symposium on VLSI (GLSVLSI), Workshop on Architectural Reliability (WAR)

Coursework

Graduate Computer Architecture, Design and Analysis of Algorithms, Advanced Computer Architecture, Parallel Computing, Advanced Data Mining, Interconnection Networks, ASIC and FPGA Design, VLSI System Design, Technological Entrepreneurship.

Undergraduate Compiler Construction, Digital System Design, Operating Systems, Formal Logic Automata Theory, Computer Network and Security, Data Mining and Warehousing, Algorithm design.

Computer Skills

Proficient Programming in: C, C++, Perl, Python

VLSI Tools: HSPICE, Mentor Graphics (Modelsim), Xilinx ISE

Familiar with Programming in: Visual C++, Intel x86 and ADSP Assembly, HTML, ASP

Architectural Simulation Tools: SimpleScalar, CACTI, HotSpot, Simflex, Simics, GEMS, M5

Personal Information

Visa Status: F1 **Country of Citizenship:** India

References

Prof. Alok Choudhary
John G. Searle Professor and Chair,
Department of EECS, and,
Applied Sciences Professor,
Kellogg School of Management,
Northwestern University
choudhar@eecs.northwestern.edu

Prof. Gokhan Memik
Associate Professor,
Department of EECS,
Northwestern University
memik@eecs.northwestern.edu

Prof. Nikos Hardavellas
June and Donald Brewer Assistant Professor,
Department of EECS,
Northwestern University
nikos@northwestern.edu

David Riss
Director Trusted Platform Research Lab,
Intel Corporation
Hillsboro, OR
david.j.riss@intel.com