

# Arindam Mallik

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Electrical Engineering and Computer Sc. Department  
Northwestern University  
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## OBJECTIVE

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Doctoral student seeking a challenging research and/or development position in the field of system design and architecture.

## RESEARCH INTERESTS

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Microarchitecture, Power & Performance Analysis, Adaptive Systems, System Design and Verification, High Performance Computing, Reliability, User-aware system design, Network Processors, Low Power Design

## ACADEMIC BACKGROUND

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- ◆ *PhD in Computer Engineering*, March 2004 – 2008  
Dissertation- “Holistic Computer Architectures based on Application, User, and Process Characteristics”  
Department of Electrical Engineering & Computer Science, Northwestern University, USA
- ◆ *MS in Computer Engineering*, September 2002- March 2004  
Thesis- “Low Power Algorithm for Optimization with Quantization Error Constraints in SystemC based ASIC Design”  
Department of Electrical & Computer Engineering, Northwestern University, USA
- ◆ *Bachelor of Computer Sc. & Engineering (First Class with honors)* August 1998 – June 2002  
Department of Computer Science & Engineering, Jadavpur University, India

## RESEARCH DETAILS

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### Doctoral Research

Dept. of EECS, Northwestern University, USA

Research Advisor: Prof. Gokhan Memik

#### *Task Allocation in Multicore Processors Using Statistical Variation [C2\*]*

- Utilizes statistical information to process network packets in multi-core processors.
- Efficient task scheduling algorithm based on statistical properties of networking applications.
- Improved scalability and utilization of processing cores in a multi-core environment.

#### *Correctness Trade-Offs in Application Specific Processors [J3, J7, C9, C11]*

- Performed Reliability-Performance Tradeoff analysis for Level-1 data cache.
- Introduced a realistic analytical model to determine the probability of a fault in a cache.
- Introduction of a new generic parameter for reliability and performance tradeoff in processors.
- Adaptive architecture to improve performance/energy consumption of application specific processors.

#### *Variable Latency Cache [C3]*

- Developed a non-uniform access Level-1 data-cache based on variability in access latency.
- Analyzed the impact of coupling and physical location on cache access latencies.

#### *User-Aware Power Management [J1, J3, C1, C4, C5, T1, P1]*

- Dynamic Voltage and Frequency Scaling in a mobile processor based on user behavior.
- Measurement of user-perceived performance and using it for DVFS.
- Prediction of user behavior based on their response to the DVFS of the system.
- Analysis of user annoyance in response to system power management.

#### *Process and Thermal-Aware Voltage Setting [J1, C4, C5, T1]*

- Explored the effect of process variation on the supply voltage of a processor.
- Analyzed the effect of operating temperature on supply voltage of a processor.
- Proposed a Dynamic Voltage Setting schema customized for individual processor and operating temperature.

#### *Low Power Caches for Network Processors [J4, C10]*

- Introduction of a new cache architecture for improved performance and reduced energy consumption in Network Processors (NPU)

\* References to relevant publications as mentioned in later sections

## Masters Research

Dept. of EECS, Northwestern University, USA

Research Advisor: Prof. Prith Banerjee

*Power Aware Architectural and Compilation Techniques Project* [J2, C6]

- Area and Power Optimization with error constraints during high level synthesis of ASIC Design.
- A new methodology for precision analysis through the combined use of simulation, high level synthesis, user input, and program analysis.

## INDUSTRY EXPERIENCE

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*Intel Corporation, Systems Technology Lab* (Hillsboro, OR, USA)

June-December, 2006

Research Intern

- Worked on many-core processor platform power modeling.
- Designed a dynamic power model for the memory subsystem.
- Proposed user-aware power management scheme for many-core ultra mobile devices.

*Cswitch Corporation* (Santa Clara, CA, USA)

June-September, 2005

Research Intern

- Involved in the design of a datapath for a reconfigurable network processor.
- Analysis of Benchmark applications in different reconfigurable logic family.

*Atrenta Inc.* (Noida, India)

June-September, 2003

Summer Intern

- Development of a Verilog compiler for the SpyGlass Predictive Analyzer software.
- Compatibility issues and benchmarking in Verilog-2001.

## JOURNAL PUBLICATIONS:

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- J1. Song Liu, Arindam Mallik, Seda O. Memik, “*An Instruction-Based Switching Model for Dynamic Power Management*”, submitted to ACM Transactions on Design Automation of Electronic Systems (ACM-TODAES)
- J2. Arindam Mallik, Gokhan Memik, “*Analyzing Correctness-Performance Trade-offs: Clumsy Packet Processors*”, submitted to ACM Transactions on Architecture and Code Optimization (ACM-TACO)
- J3. Arindam Mallik, Debjit Sinha, Prith Banerjee, and Hai Zhou, “*Low Power Optimization by Smart Bit-width Allocation in a SystemC based ASIC Design Environment*”, IEEE Transactions on Computer-aided Design of Integrated Circuits and System (IEEE-TCAD), Volume 26, Number 3, March 2007
- J4. Arindam Mallik, Bin Lin, Gokhan Memik, Peter Dinda, Robert P. Dick, “*User-Driven Frequency Scaling*”, IEEE Computer Architecture Letters (IEEE-CAL), Volume 5, no. 2, 2006
- J5. Arindam Mallik and Gokhan Memik “*Low Power Correlating Caches for Network Processors*”, Published in The Journal for Low Power Electronics (JOLPE). Volume 1, Number 2, August 2005
- J6. Arindam Mallik, M. Wildrick and Gokhan Memik, “*Application-Level Error Measurements for Network Processors*”, In Institute of Electronics, Information and Communication Engineers Transactions on Information and Systems (IEICE-TIS), Volume E88-D, Number 8, August 2005

## CONFERENCE PUBLICATIONS:

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- C1. Alex Shye, Berkin Ozisikyilmaz, Arindam Mallik, Gokhan Memik, Peter Dinda, Robert Dick, Alok Choudhary, “*Learning and Leveraging the Relationship between Architecture-Level Measurements and Individual User Satisfaction Scaling*”, submitted in The 35th International Symposium on Computer Architecture (ISCA-2008)
- C2. Arindam Mallik, Jack Cosgrove, Gokhan Memik, Robert P. Dick, Peter Dinda, “*PICSEL: Measuring User-Perceived Performance to Control Dynamic Frequency Scaling*”, in The International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-2008)
- C3. Arindam Mallik, Yu Zhang and Gokhan Memik, “*Automated Task Distribution in Multicore Network Processors using Statistical Analysis*”, in The Symposium on Architectures for Networking and Communications Systems (ANCS-2007)
- C4. Serkan Ozdemir, Arindam Mallik, Ja Chun Ku, Gokhan Memik, Yehea Ismail, “*Variable Latency Caches using Access Time Prediction for Nanoscale Processors*”, in The International Conference for High Performance Computing, Networking, Storage and Analysis (SC-2007), winner of the best student paper
- C5. Peter Dinda, Gokhan Memik, Robert P. Dick, Bin Lin, Arindam Mallik, Asish Gupta, and Samuel Rossoff, “*The User in Experimental Computer Systems Research*”, in the Workshop on Experimental Computer Science in conjunction with The Federated Computer Research Conference (FCRC-2007), June 2007, California, USA
- C6. Bin Lin, Arindam Mallik, Gokhan Memik, Peter Dinda, Robert P. Dick, “*Power Reduction Through Measurement and Modeling of Users and CPUs*”, in the Proc. of International Conference on Measurement and Modeling of Computer Systems (ACM SIGMETRICS-2007), June 2007, California, USA

- C7. Arindam Mallik, Debjit Sinha, Prith Banerjee, Hai Zhou, “*Smart Bit-width Allocation for Low Power Optimization in a SystemC based ASIC design Environment*”, in the Proc. of Design, Automation and Test in Europe (DATE-2006), March 2006, Munich, Germany
- C8. Gokhan Memik, Masud H. Chowdhury, Arindam Mallik, Yehea I. Ismail, “*Engineering Over-Clocking: Reliability-Performance Trade-Offs for High-Performance Register Files*”, in the Proc. of International Conference on Dependable Systems and Network (DSN-2005), June, 2005, Yokohama, Japan
- C9. Gokhan Memik, Mahmut T. Kandemir, Arindam Mallik, “*Load Elimination for Low-Power Embedded Processors*”, in the Proc. of Great Lakes Symposium on VLSI 2005 (GLSVLSI-2005), April 2005, Chicago, IL
- C10. Arindam Mallik and Gokhan Memik, “*A Case for Clumsy Packet Processors*”, in the Proc. of International Symposium on Microarchitecture (MICRO-2004), December 2004, Portland, OR
- C11. Arindam Mallik and Gokhan Memik, “*Design and Study of Correlation Cache*”, in the Proc. of International Symposium on Low Power Electronic Design (ISLPED-2004), August 2004, Newport Beach, CA
- C12. Arindam Mallik, Matthew Wildrick, Gokhan Memik, “*Measuring Application Error Rates for Network Processors*”, in the Proc. of Intl. Midwest Symposium on Circuits and Systems (MWSCAS-2004), July 2004, Hiroshima, Japan

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### TECHNICAL REPORT:

- T1. Arindam Mallik, Bin Lin, Peter Dinda, Gokhan Memik, and Robert P. Dick, “*Process and User Driven Dynamic Voltage and Frequency Scaling*”, Technical Report NWU-EECS-06-11, Department of Electrical Engineering and Computer Science, Northwestern University, August, 2006

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### PATENTS:

- P1. Peter Dinda, Gokhan Memik, Robert P. Dick, Arindam Mallik, and Bin Lin, “*Process and User Driven Dynamic Voltage and Frequency Scaling*”, under Northwestern University Technology Transfer Program, November 2006.

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### KEY SKILLS

- Programming Languages: C, Perl, C++, Windows batch scripts, Verilog, SystemC
- Architectural Simulation Framework: SimpleScalar Simulator, CACTI, Click modular router, Intel PLATO
- Software Tools: gcc, gdb, Visual Studio, Microsoft .NET Framework Software Development Kit, flex, bison
- EDA Tools: Cocentric SystemC Compiler, Synopsys Design Compiler, Mentor Graphics tools

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### HONORS AND AWARDS:

- Recipient of the “*Royal E. Cabell Fellowship*” award on year 2006-07 for terminal year of Doctoral thesis dissertation by The Graduate School, Northwestern University.
- Recipient of the “*Walter P. Murphy Fellowship*” award on year 2002 by the Robert R McCormick School of Engineering and Applied Science, Northwestern University.
- Recipient of the *National Scholarship* from year 1996-2002 under the National Talent Search Scheme, India.

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### REVIEWER:

- DAC, DSN, EUC, GLSVLSI, ISCA, ISPASS, IISWC

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### EXTRA CURRICULAR ACTIVITIES:

- Serves as a panel member in the InNUvation, Northwestern University student entrepreneur’s panel.
- Executive committee member of Graduates in Electrical Engg. & Computer Sc. (GEECS) at Northwestern University.

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### AFFILIATIONS:

- Member of IEEE; Member of IEEE Computer Society; Member of ACM-SIGARCH

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### REFERENCES:

Prof. Gokhan Memik (Advisor)  
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