

Alex Shye

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shye@northwestern.edu

- RESEARCH INTERESTS
- User-aware computer architectures and systems
 - Run-time profiling and optimization systems
 - Software-implemented fault tolerance
 - Computer architecture and systems in general
- EDUCATION
- Northwestern University** – Evanston, IL 2007–present
Pursuing PhD degree in Electrical and Computer Engineering
- Advised by Professor Gokhan Memik
- University of Colorado** – Boulder, CO 2005–2007
PhD student in Computer Engineering
- University of Colorado** – Boulder, CO 2003–2005
MS degree in Computer Engineering
- Advised by Professor Daniel A. Connors
- University of Illinois** – Urbana-Champaign, IL 1998–2002
BS degree in Computer Engineering
- ACADEMIC EXPERIENCE
- Northwestern University** – Evanston, IL Fall 2007–present
Research Assistant
- Involved in ESP: Empathic Systems Project
- Exploring novel methods of incorporating the user for optimizing architectures
- University of Colorado** – Boulder, CO Spring 2006, Spring 2007
Research Assistant
- Research on software-implemented transient fault tolerance
- TEACHING EXPERIENCE
- Northwestern University** – Evanston, IL Winter 2008
Teaching Assistant
- Hold recitation, creating programming assignments, hold office hours and grade assignments/tests
- University of Colorado** – Boulder, CO Fall 2004, Spring 2005
Teaching Assistant
- Lead two lab sections in assembly programming course for the Motorola 68000, hold office hours, and grade assignments.
- INDUSTRY EXPERIENCE
- Advanced Micro Devices Inc.** – Boxborough, MA Summer 2008–present
Computing Solutions Group – Co-op
- Work on development of a dynamic optimization system.
- Manager: Joyce Spencer
- Google Inc.** – Mountain View, CA Summer 2007
Cluster Performance Analysis Group – Summer Intern
- Develop a profiling tool for finding the dynamic allocation site of cache misses to dynamically allocated data using a combination of hardware performance monitoring samples and binary analysis
- Manager: Brad Chen
- Intel Corporation** – Nashua, NH Summer–Fall 2006
Dynamic Optimization Laboratory – Intern
- Develop a profile-directed dynamic memory allocator that uses allocation information and memory reference behavior to choose between specialized memory allocators
- Manager: John Pieper
- IBM T.J. Watson Research Center** – Yorktown Heights, NY Summer 2005
Programming Models and Tools for Scalable Systems – Summer Intern
- Explored locality in data reference streams using large pages with dynamic memory allocation
- Manager: Calin Cascaval, Mentor: Evelyn Duesterwald

- JOURNAL PUBLICATIONS [J1] Alex Shye, Joseph Blomstedt, Tipp Moseley, Vijay Janapa Reddi, and Daniel A. Connors. **PLR: A Software Approach to Transient Fault Tolerance for Multi-Core Architectures**. *IEEE Transactions on Dependable and Secure Computing (TDSC)*. Accepted for publication.
- CONFERENCE PUBLICATIONS [C1] Alex Shye, Yan Pan, Ben Scholbrock, J. Scott Miller, Gokhan Memik, Peter A. Dinda, and Robert P. Dick. **Power to the People: Leveraging Human Physiological Traits to Control Microprocessor Frequency**. In *proceedings of the 41st IEEE/ACM International Symposium on Microarchitecture (MICRO)*. Lake Como, Italy. November 8-12, 2008. Acceptance Rate: 19.0% (40/210)
Best Paper Award Nominee (Top 8 papers selected by PC)
- [C2] Alex Shye, Berkin Ozisikyilmaz, Arindam Mallik, Gokhan Memik, Peter A. Dinda, Robert P. Dick, and Alok N. Choudhary. **Learning and Leveraging the Relationship between Architecture-Level Measurements and Individual User Satisfaction**. In *proceedings of the 35th ACM/IEEE International Symposium on Computer Architecture (ISCA)*. Beijing, China. June 21-25, 2008. Acceptance Rate: 14.3% (37/259)
- [C3] Alex Shye, Lei Yang, Xi Chen, Berkin Ozisikyilmaz, Arindam Mallik, Bin Lin, Gokhan Memik, Peter A. Dinda, and Robert P. Dick. **Empathic Computer Architectures and Systems**. In *the 13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems: Wild and Crazy Ideas Session (ASPLOS WACI)*. Seattle, WA. March 3, 2008. Acceptance Rate: 40%
- [C4] Dan Fay, Alex Shye, Sayantan Bhattacharyya, Steve Wichmann and Daniel A. Connors. **An Adaptive Fault-Tolerant Memory System for FPGA-based Architectures in the Space Environment**. In *proceedings of the 3rd NASA/ESA Conference on Adapative Hardware Systems (AHS)*. Edinburgh, UK. August 5-8, 2007.
- [C5] Alex Shye, Tipp Moseley, Vijay Janapa Reddi, Joseph Blomstedt and Daniel A. Connors. **Using Process-Level Redundancy to Exploit Multiple Cores for Transient Fault Tolerance**. In *proceedings of the 37th IEEE/IFIP International Conference on Dependable Systems and Networks (DSN)*. Edinburgh, UK. June 25-28, 2007. DCCS Session Acceptance Rate: 25.0% (53/212)
- [C6] Tipp Moseley, Alex Shye, Vijay Janapa Reddi, Dirk Grunwald and Ramesh Peri. **Shadow Profiling: Hiding Instrumentation Costs with Parallelism**. In *Proceedings of the IEEE/ACM International Symposium on Code Generation and Optimization (CGO)*. San Jose, CA. March 11-14, 2007. Acceptance Rate: 32.1% (27/84).
Runner-up for Best Paper Award (Voted by conference attendees)
- [C7] Alex Shye, Matthew Iyer, Vijay Janapa Reddi, Daniel A. Connors. **Code Coverage Testing Using Hardware Performance Monitoring Support**. In *proceedings of the 6th ACM International Symposium on Automated and Analysis-Driven Debugging (AADEBUG)*. Monterey, CA. September 19-21, 2005. Acceptance Rate: 60.0% (18/30)
- [C8] Tipp Moseley, Alex Shye, Vijay Janapa Reddi, Matthew Iyer, Dan Fay, Dave Hodgdon, Joshua L. Kihm, Alex Settle, Dirk Grunwald, Daniel A. Connors. **Dynamic Run-time Architecture Techniques for Enabling Future Multithreaded Multiprocessors**. In *proceedings of the 2nd ACM International Conference on Computing Frontiers (CF)*. Ischia, Italy. May 4-6, 2005. Acceptance Rate: 40.6% (43/106)
- WORKSHOP PUBLICATIONS [W1] Alex Shye, Vijay Janapa Reddi, Tipp Moseley, Daniel A. Connors. **Transient Fault Tolerance via Dynamic Process-Level Redundancy**. In *proceedings of the 2nd Workshop on Binary Instrumentation and Applications in conjunction with ASPLOS-XII (WBIA)*. San Jose, CA. October 21-25, 2006.
- [W2] Alex Shye, Matthew Iyer, Tipp Moseley, David Hodgdon, Dan Fay, Vijay Janapa Reddi, Daniel A. Connors. **Analysis of Path Profiling Information Generated with Performance Monitoring Hardware**. In *proceedings of the 9th Workshop on Interaction between Compilers and Computer Architecture in conjunction with HPCA-11 (INTERACT)*. San Francisco, CA. February 12-14, 2005.
- TECHNICAL REPORTS [TR1] Alex Shye. **Exploring the Potential of Performance Monitoring Hardware to Support Run-time Optimization**. *M.S. Thesis*. Department of Electrical and Computer Engineering, University of Colorado. May, 2005.
- TALKS/POSTERS [T1] **Power to the People: Leveraging Human Physiological Traits to Control Micropro-**

cessor Frequency. *41st IEEE/ACM International Symposium on Microarchitecture (MICRO)*. Lake Como, Italy. November 11, 2008.

[T2] **Learning and Leveraging the Relationship between Architecture-Level Measurements and Individual User Satisfaction.** *35th ACM/IEEE International Symposium on Computer Architecture (ISCA)*. Beijing, China. June 25, 2008.

[T3] **Empathic Computer Architectures and Systems.** *13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems: Wild and Crazy Ideas Session (ASPLOS-WACI)*. Seattle, WA. March 3, 2008.

[T4] **Using Process-Level Redundancy to Exploit Multiple Cores for Transient Fault Tolerance.** *37th IEEE/IFIP International Conference on Dependable Systems and Networks (DSN)*. Edinburgh, UK. June 27, 2007.

[T5] **SNAKES: A Software Framework for Transparent, Replica-based, Transient Fault Tolerance.** *ACM Student Research Competition held at PLDI 2007 Poster Session in conjunction with FCRC/PLDI (ACM-SRC)*. San Diego, CA. June 10, 2007.

[T6] **Attack of the Clones: Using Process Replicas in Multi-core Systems.** *Invited talk at Front Range Architecture Compilers Tools and Languages Workshop (FRACTAL)*. Fort Collins, CO. February 10, 2007.

[T7] **Transient Fault Tolerance via Dynamic Process-Level Redundancy.** *2nd Workshop on Binary Instrumentation and Applications in conjunction with ASPLOS-XII (WBIA)*. San Jose, CA. October 22, 2006.

[T8] **Code Coverage Testing Using Hardware Performance Monitoring Support.** *6th ACM International Symposium on Automated and Analysis-Driven Debugging (AADEBUG)*. Monterey, CA. September 21, 2005.

[T9] **Analysis of Path Profiling Information Generated with Performance Monitoring Hardware.** *9th Workshop on Interaction between Compilers and Computer Architecture in conjunction with HPCA-11 (INTERACT)*. San Francisco, CA. February 13, 2005.

AWARDS

Nominee, Best Paper Award – MICRO 2008 (Top 8 papers selected by PC)
Runner-up, Best Paper Award – CGO 2007 (Voted by conference attendees)
Recipient, Walter P. Murphy Fellowship – Northwestern University 2007

PROFESSIONAL ACTIVITIES

External Reviewer:

- International Conference on Computer Design (ICCD) - 2005
- International Symposium on Code Generation and Optimization (CGO) - 2006, 2007
- Workshop on Interaction between Compilers and Computer Architectures (INTERACT) - 2006
- Symposium on Applied Computing - Track on Embedded Systems (SAC EMBS) - 2008, 2009
- Great Lakes Symposium on VLSI (GLSVLSI) - 2008
- Design, Automation, and Test in Europe (DATE) - 2009
- IEEE Transactions on Embedded Computing Systems - 2006
- IEEE Transactions on Computers - 2008

Organizer, Northwestern Grads in EECS (GEECS) - 2007–present
Student member, IEEE, ACM, ACM SIGPLAN, ACM SIGARCH

MISCELLANEOUS

Citizen of the United States of America.
References available upon request.
For more information, please visit my webpage: <http://www.ece.northwestern.edu/~ash451>