

Debasish Das

M314, Technological Institute
Department of Electrical Engineering and Computer Science
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Interests

1. Static timing analysis, Gate Sizing, Statistical optimization
2. Mathematical modeling of VLSI
3. Reconfigurable logic: Power and Timing issues in FPGA

Education

Doctoral in Computer Engineering (Currently Pursuing)
Department of Electrical and Computer Engineering,
Robert R McCormick School of Engineering & Applied Sciences,
Northwestern University, Evanston, USA

Bachelor of Technology (B.Tech, Hons) (2004)
Department of Computer Science and Engineering,
Indian Institute of Technology, Kharagpur, India

Research & Training Experience

Graduate Student

Department of Electrical Engineering and Computer Science.
Northwestern University, Evanston, USA
March 2005 - Present

Research Advisor - *Prof. Hai Zhou*

Projects:

1. Static Timing Analysis with Crosstalk effects: Considering parasitic effects such as crosstalk, the present approaches to timing analysis is time consuming. This project deals with developing speed-up techniques to do timing analysis taking into account the crosstalk effects that are bound to appear in deep submicron technologies. Complex timing and coupling models are explored in this project to get realistic timing analysis for 90nm technology nodes and beyond. Relevant papers : [2,3]
Collaborators:
 1. Strategic CAD Lab, Intel Corporation, USA
 2. High performance IC Design and Analysis Lab, Northwestern University, Evanston
 3. Faraday Technology
2. Accurate and efficient gate sizing: Traditional gate sizing ignored the impact of gate size alteration on the timing properties of each arc associated with the gate. In this research we develop models to capture the timing information in gate sizing accurately. We are developing efficient flow based solver for sub-gradient computation in traditional LR-based gate sizing.

3. Timing Analysis of un-buffered sequentials: Un-buffered latches are key elements of modern day high performance microprocessor design due to their property to lower delay and power consumption. This research explores the effect of un-buffered sequentials on performance verification and timing optimization.
4. Statistical Optimization: As a course project I extended the linear delay model used for statistical timing analysis to a quadratic model and found closed form solutions for the quadratic model to be used in Statistical Timing Analysis framework. Future direction of this project will involve statistical optimization considering crosstalk.

September 2004 - February 2005

Project Advisor - *Prof. Seda Memik*

Project:

1. Power Aware Reconfigurable Logic: This project proposed an approach to save the leakage power in FPGAs. Relevant paper : [1]
2. Analysis of Routing Pattern of FPGAs: I developed a tool based on VPR for the analysis of routing patterns in FPGAs. Please refer my website for the source code.

Graduate Summer Intern

Strategic CAD Lab, Intel Corporation.

Hillsboro, Oregon, USA

June 2006 - September 2006

Project Advisors - Kip Killpack and Dr. Chandramouli Kashyap

Manager - Dr. Noel Menezes

Project: This project presented a novel iterative algorithm for pessimism reduction in static timing analysis in presence of crosstalk using logic and timing filtering. An accurate coupling model based on arrival times and slews is presented which invalidates the monotonic property of Miller Coupling Factor computation as claimed by earlier research. In this research we also derive a sensitivity based metric to select aggressors for logic analysis as logic analysis is often run-time inefficient. Relevant paper: [4]

Graduate Summer Intern

Calypto Design Systems Inc.

San Jose, California, USA

June 2005 - September 2005

Project Advisors - Rajat Subhra Mukerjee, Abhishek Ranjan, Dr. Sumit Roy and Dr. Venky Ramachandran

Projects:

1. Enhancements to SLEC Optimization engine like propagating constants across different types, optimization of scan-latch designs and strength reductions.
2. For timing analysis of system level designs, fast generation of accurate timing macromodel for system level blocks are essential. I developed an efficient

timing macromodeling algorithm for word level static timing analysis. The algorithm is integrated to the static timer at Calypto. Relevant paper : [5]

B.Tech Senior Year Student

Department of Computer Science and Engineering
Indian Institute of Technology, Kharagpur, India
August 2003-May 2004

Project Advisor - *Prof. Anupam Basu and Prof. Arobinda Gupta*

This project dealt with developing text-to-speech synthesis software called Embedded Shurti for handheld devices running Windows CE. This extended the Shruti software developed by MediaLab, IIT Kharagpur into the domain of Pocket-PCs.

Undergraduate Summer Intern

Tata Research Design and Development Centre
Tata Consultancy Services, Pune, India

May 2003-July 2003

Project Advisor - *Dr. Prahlad Sampath*

Developed a binary decision diagram solver to solve live variable analysis of high level languages.

B.Tech Junior Year Student

Department of Computer Science and Engineering
Indian Institute of Technology, Kharagpur, India
May 2002-May 2003

1. Advanced VLSI Laboratory, Indian Institute of Technology, Kharagpur
16th Dec 2002- 20th Dec 2002

Attended a course on Advanced Computer Architecture by *Prof. Trevor Mudge*, University of Michigan at Ann Arbor.

2. Continuing Education Program, Indian Institute of Technology, Kharagpur
22nd May 2002-7th June 2002

Attended a course on Object Oriented Programming in C++ and Visual C++ conducted by Mathematics department, IIT Kharagpur and secured an EX (Excellent) grade.

Associated faculty: Dr. D Goswami

Referred Publications:

1. Somsubhra Mondal, Debasish Das and Seda Memik. Hierarchical LUT Structures for Leakage Power Reduction, Poster Paper, Proc. International Symposium on FPGAs (FPGA 2005), Monterey, CA, USA.
2. Debasish Das, Ahmed Shebaita, Hai Zhou, Yehea Ismail and Kip Killpack. FA-STAC: A Framework for Fast and Accurate Static Timing Analysis with Coupling, IEEE International Conference on Computer Design, San Jose, CA, 2006.
3. Debasish Das, Ahmed Shebaita, Yehea Ismail, Hai Zhou and Kip Killpack. Nostra-XTalk: A Predictive Framework for Accurate Static Timing Analysis in UDSM VLSI Circuits, ACM Great Lakes Symposium on VLSI, Stresa, Italy, 2007.
4. Debasish Das, Kip Killpack, Chandramouli Kashyap, Abhijit Jas and Hai Zhou. Pessimism Reduction in Coupling Aware Static Timing Analysis Using Timing and Logic Filtering, Submitted to Design Automation Conference, 2007.

Non-referred Publications:

5. Debasish Das, Abhishek Ranjan, Sumit Roy and Venky Ramachandran, Efficient Timing Macromodeling for Word Level Static Timing Analysis, Internal Report, Calypto Design Systems Inc.
6. Debasish Das, Symbolic solver for live variable analysis of high level design languages, accepted to IEEE Computer Society Annual Symposium on VLSI, Karlsruhe, Germany, 2006.

Scores

GRE: Quantitative: 800/800 Verbal: 550/800 Analytical: 4.5/6.0
TOEFL: 270/300, TSE: 45/60

Relevant Courses

Graduate Courses (GPA = 3.9/4.0)

Electrical Engineering and Computer Science Courses: Computer Architecture, VLSI System Design, Introduction to VLSI CAD, Design and Analysis of High Speed ICs, Formal Techniques in Design and Verification of Digital Systems, Design and Analysis of Algorithms, Advanced Algorithms, Seminar on Computer Security and Information Assurance, Random Processes in Communications and Control - I, Advanced Computer Architecture - II, Numerical Methods for Engineers

Industrial Engineering and Management Sciences Courses: Mathematical Programming

Undergraduate Courses (GPA = 8.3/10.0)

Departmental Core: Programming and Data Structure, Discrete Structures, Switching Circuits and Logic Design, Design and Analysis of Algorithms, Computer Organization and Architecture, Formal Language and Automata Theory, Operating Systems, Computer Networks.

Departmental Electives: Microprocessors and Microcontrollers, Software Engineering, Electronic Design Automation, Artificial Intelligence, Compiler Construction, VLSI System Design, Embedded Systems, Applied Graph Theory, Low power circuits and systems, File Organization and Database Systems.

Other subjects: Basic Electronics, Electrical Technology, Electromagnetic Engineering, Semiconductor Devices, Probability and Statistics, Signals and Networks, Linear Algebra.

Fellowship and Achievements

1. Awarded travel grant to participate in Design Automation Summer School (DASS 2005) held in conjunction with Design Automation Conference, Anaheim, CA, USA 2005.
2. Walter P Murphy Fellowship awarded by the Department of Electrical and Computer Engineering, Robert R McCormick School of Engineering & Applied Sciences, Northwestern University for 2004-2005.
3. Was among the top 0.1% of students selected in IIT-JEE examinations (to get admission into Indian Institute of Technology).
4. Awarded merit certificate under National Scholarship Scheme from Director of Education, Government of India for outstanding performance in SSE Examinations.

Technical Skills

1. Languages: C, C++, Java, Visual C++, VHDL/Verilog
2. Tools: AMPL, CPLEX, TLA+, Mentor Graphics EDA Suite, Synopsys DC, gdb, lex, yacc, gcc

Additional Activities

1. Reviewer: TCAD, DAC, ICCAD, ISPD, ISQED, TAU, VLSI India
2. Teaching Assistant for ECE203 (Introduction to Computer Engineering) Fall, Spring 2005, ECE231 (Advanced Programming for Computer Engineers) Winter 2006, ECE357 (Introduction to VLSI CAD) Fall 2006, EECS366 (Design and Analysis of Algorithms) Winter 2006.
3. Member of Bitwise 2004 organizing committee; Bitwise is an annual online Programming contest organized by the Department of Computer Science and Engineering, IIT Kharagpur.
4. Awarded 'B' level certificate from National Cadet Corps, India.

References (Email address will be furnished upon request)

Professor Hai Zhou,
Department of EECS,
Northwestern University, USA

Professor Yehea Ismail,
Department of EECS,
Northwestern University, USA

Dr. Sumit Roy,
Head of Engineering,
Calypto Design Systems Inc, USA

Kip Killpack,
Strategic CAD Lab
Intel Corporation, USA

Professor Ajit Pal,
Department of Computer Science and Engg,
Indian Institute of Technology, Kharagpur, India