Northwestern University
Electrical Engineering and Computer Science
EECS 303: Advanced Digital Design, Fall 11
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Handout #9
Due: Nov 8

**Lab 3 Speed Up GCD Computer**

In this lab, we are going to speed up the GCD computer we designed in lab 2. There are at least two ideas for speeding up our design. The first one is to deploy the carry look-ahead circuit in place of the original ripple carry design. The second is to reduce the number of iterations when the difference between the two numbers is huge. We only pursue the first idea in this assignment.

# 1 Simulation With Delays and Clock Period

The first task in this lab is to assign a delay to each block in your GCD computer in Lab 2 and simulate the circuit with delays. Here, we need to set up the delay for each block in Design Architect to 10ns. The two zeroes beside each block on the schematic indicate its output rising and falling delay in nanoseconds. To assign 10ns rising and falling delay to each block:

1. From the main menu bar:
   Setup → Select Filter...

   A dialog box will appear. Click on Clear All. Select Properties only. Then click OK
2. Select the two 'zeroes' beside the gate.
3. Select 'TEXT' on the right hand side schematic palette. The palette will be refreshed.
4. Select 'CHANGE VALUE' on the palette. A dialog bar will appear on the bottom. Enter 10 in the new value box for rising delay and click OK. The zero beside the gate will become '10'.
5. Also enter 10 in the new value box for falling delay and click OK.

To simulate with QuickSim using actual gate delays, click TIMING MODE from the SETUP palette. This will bring up a window to allow selection of timing analysis. Click All, Change → Full Delays Typ and click OK. Then the simulation will include the delays.

Please use 40ns as clock period for a simulation, observe what you get on the waveforms.

Please use calculation to find the minimal working clock period for your GCD computer. Set the clock period according to your calculation, and simulate the circuit for the 3 instances in Lab 2.

# 2 Speed up GCD by Carry Look Ahead Circuit

The second task of the lab is to design and deploy a carry look ahead circuit to speed up your GCD computer. First, design a 4-bit carry look ahead circuit and input it into the design architect. Please also set up its delay to be 10ns.

Now you can connect the carry look ahead circuit to your GCD computer. Please calculate the minimal clock period for the new machine, and simulate it for the 3 instances in Lab 2.

# 3 Report

Please report the schematics of your design, and simulation traces. There should be 7 traces: 1 trace of 40ns clock period, and 3 traces of min clock period, on old GCD; 3 traces of min clock period on new GCD.