Northwestern University
Electrical Engineering and Computer Science
EECS 303: Advanced Digital Design
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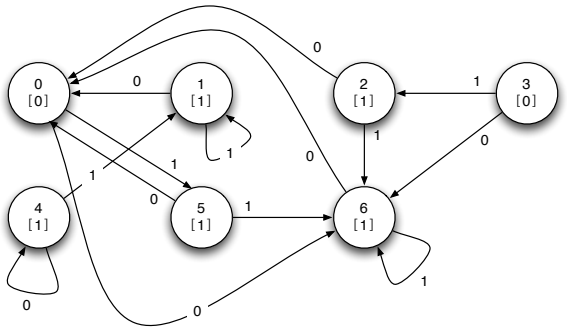
Handout #

Midterm Examination

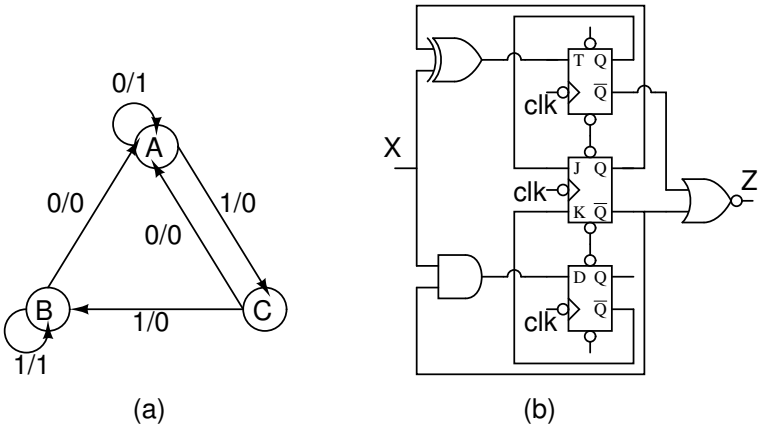
Name:_____ **ID:**_____

There are six problems. Be precise, show every step, and state your assumptions (if any), to get full credit.

1. (10 pts) Decide whether the following statements are true or false:
   (a) Similar to Quine-McCluskey method, Espresso method can be used to find an optimal solution for 2-level logic.
   (b) Any finite state machine can be implemented by using only NOR gates.
   (c) A Moore machine requires a clock signal, while a Mealy machine does not.
   (d) In RS latch, the input "11" is forbidden since the next state is uncertain.
   (e) After state minimization, a finite state machine will have a unique logic diagram.
2. (10 pts) Implement the minimized form of the following logic expression.
$$F(A,B,C,D) = \sum m(3,6,7,9,11,12,13) + d(14,15)$$
   (a) Use a two-level NAND-NAND gate network.
   (b) Use a two-level NOR-NOR gate network.
3. (20 pts) Use the Quine-McClusky method to find the minimized sum of products expression for the function $F(a,b,c,d) = \sum m(1,5,7,8,9,13,15) + d(4,14)$. You must show your work.
4. (20 pts) Starting with the following state graph, use the implication chart method to find the minimum state graph. Which states in the orginal graph are equivalent?



5. (20 pts) Implement the state machine in (a) with D flip-flops; and give the state graph for the circuit in (b).



6. (20 pts) A sequential circuit has two inputs and two outputs. The inputs (X_1, X_2) represent a 2-bit binary number, N. If the present value of N is greater than the previous value, then $Z_1 = 1$. If the present value of N is less than the previous value, then $Z_2 = 1$. Otherwise, Z_1 and Z_2 are 0. Design a Mealy machine for the circuit and show every step of your design.