Hai Zhou

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Department of Electrical Engineering and Computer Science
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Current Position

NORTHWESTERN UNIVERSITY — Evanston, IL
2007 – present. Associate Professor of Electrical Engineering and Computer Science.
2005 – 2007. Assistant Professor of Electrical Engineering and Computer Science.
2001 – 2005. Assistant Professor of Electrical and Computer Engineering.

Education

THE UNIVERSITY OF TEXAS — Austin, TX
Ph.D. in Computer Sciences, May, 1999.
Ph.D. Thesis: "Signal Integrity and Low Power Issues in Deep Sub-Micron VLSI Design".
Advisor: Prof. Martin D. F. Wong.

TSINGHUA UNIVERSITY — Beijing, China
M.E. in Computer Science and Technology, June, 1994.

TSINGHUA UNIVERSITY — Beijing, China
B.E. in Computer Science and Technology, June, 1992.

Main Research Interests

- VLSI physical design automation.
- Statistical timing analysis and optimization.
- Timing optimization of sequential circuits.
- Interconnect optimization.
- Formal algorithm design methodology.

Experience

SYNOPSYS INC. — Mountain View, CA
6/99–8/01. Senior R&D Engineer, Advanced Technology Group.

AVANTI CORP. — Fremont, CA
6/97–8/97. Summer Intern, Placement and Routing Group.

THE UNIVERSITY OF TEXAS — Austin, TX
8/94–6/99. Research/Teaching Assistant, Department of Computer Sciences, Department of Electrical and Computer Engineering.

Professional Activities

- Associate Editor, *ACM Transactions on Design Automation*, 2008 - present.
- Associate Editor, *Integration, the VLSI Journal*, 2008 - present.
- Editorial Board, *Integration, the VLSI Journal*, 2006 - 2008.
- Area Editor of "VLSI CAD algorithms", *The Encyclopedia of Algorithms*, a book that will be published by Springer in 2007.
- Member of Technical Program Committee, *ACM Design Automation Conference (DAC) 2008*

- General Co-Chair, *ACM Great Lakes Symposium on VLSI (GLSVLSI) 2007*
- Member of Technical Program Committee, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2007*
- Member of Technical Program Committee, *ACM Design Automation Conference (DAC) 2007*
- Member of Technical Program Committee, *ACM International Symposium on Physical Design (ISPD) 2007*
- Co-Chair of Technical Program Committee, *ACM Great Lakes Symposium on VLSI (GLSVLSI) 2006*
- Member of Best Paper Award Committee, Member of Technical Program Committee, *ACM/IEEE Design Automation Conference (DAC) 2006*
- Member of Technical Program Committee, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2006*
- Co-Chair, Local Arrangements, Member of Technical Program Committee, *ACM Great Lakes Symposium on VLSI (GLSVLSI) 2005*
- Member of Technical Program Committee, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2005*
- Member of Technical Program Committee, *ACM Asia South Pacific Design Automation Conference (ASP-DAC) 2005*
- Member of Technical Program Committee, *ACM International Symposium on Physical Design (ISPD) 2005*
- Member of Technical Program Committee, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2004*
- Member of Technical Program Committee, *IEEE International Conference on Computer Design (ICCD) 2004*
- Member of Technical Program Committee, *ACM Great Lakes Symposium on VLSI (GLSVLSI) 2004*
- Member of Technical Program Committee, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2003*
- Publications Chair, *ACM Great Lake Symposium on VLSI (GLSVLSI) 2003*
- Member of Technical Program Committee, *ACM International Symposium on Physical Design (ISPD) 2002*
- Member of Technical Program Committee, *ACM International Symposium on Physical Design (ISPD) 2001*
- Member of Technical Program Committee, *ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (Tau) 2004, 2005, 2006*
- Panelist of National Science Foundation peer review panel, 2003, 2006
- Proposal reviewer, University of California MICRO Program, 2005, 2006
- Chairs of various sessions, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD), ACM International Symposium on Physical Design (ISPD), ACM Asia-South Pacific Design Automation Conference (ASP-DAC)*

Honors and Awards

- ACM SIGDA Technical Leadership Award, 2008
- ACM Service Award, 2007
- NSF CAREER Award, 2003
- Senior Member, IEEE, 2004
- Synopsys Special Recognition Award (for excellent performance and outstanding contribution to Synopsys Engineering), 2000

- Tsinghua University Outstanding Graduate Award, 1994

Funding

[F1] "CPA-DA: Efficient Sequential Synthesis and Optimization for High-Performance Circuits," PI, *National Science Foundation*, 9/1/08-8/31/11.

[F2] "Thermal-Aware Unified Architectural and Physical Design of Reliable Integrated Systems," Co-PI (with R. Dick (EECS, Northwestern) and L. Shang (ECE, Queen's University)), *Semiconductor Research Corporation*, 4/1/07–3/31/10.

[F3] "SoD-Team: Robust System Design Under Weak Component Assumptions," PI (with R. Dick and A. Choudhary (EECS, Northwestern)), *National Science Foundation*, 9/1/06-8/31/08.

[F4] "CAREER: Formal Methods for Silicon Complexity in Nanometer VLSI Design," PI, *National Science Foundation*, 2/1/03–1/31/08.

[F5] "REU Supplement to CAREER: Formal Methods for Silicon Complexity in Nanometer VLSI Design," PI, *National Science Foundation*, 2006.

[F6] "Speeding up Static Timing Analysis with Crosstalk," PI, *Intel*, 4/1/05–3/31/08.

[F7] "Adaptive Intrusion Detection and Mitigation Systems for WiMAX Networks," Co-PI (with Y. Chen (EECS, Northwestern)), *Motorola Center for Seamless Communications*, 9/1/06-8/31/07.

[F8] "Data Flow Driven Floorplanning," PI, *Cadence Design Systems*, 1/1/05-12/31/05.

[F9] "Equipment Grant for Timing Analysis Research," PI, *Intel*, 2005.

Publications

Chapters in Book

[B1] H.-M. Chen, D. F. Wong, H. Zhou, F. Y. Young, H. H. Yang, and N. Sherwani. "Integrated Floorplanning and Interconnect Planning", in *Layout Optimizations in VLSI Designs*, B. Lu, D.-Z. Du, and S. Sapatnekar eds., Kluwer Academic Publishers. 2002.

[B2] D. Mehta and H. Zhou, "Basic Data Structures", in *Handbook of Algorithms for Physical Design Automation*, C. Alpert, D. Mehta, and S. Sapatnekar eds., CRC Press. 2007.

[B3] H. Zhou, "Rectilinear Spanning Tree (2002; Zhou, Shenoy, Nicholls)" in *Encyclopedia of Algorithms*, M.-Y. Kao eds., Springer. 2008.

[B4] H. Zhou, "Circuit Retiming (1991; Leiserson and Saxe)" in *Encyclopedia of Algorithms*, M.-Y. Kao eds., Springer. 2008.

[B5] H. Zhou, "Rectilinear Steiner Tree (2004; Zhou)" in *Encyclopedia of Algorithms*, M.-Y. Kao eds., Springer. 2008.

[B6] H. Zhou, "Circuit Retiming: An Incremental Approach (2005; Zhou)" in *Encyclopedia of Algorithms*, M.-Y. Kao eds., Springer. 2008.

Journal (In Print or In Press)

[J1] H. Zhou and D. F. Wong. Optimal River Routing with Crosstalk Constraints. *ACM Transactions on Design Automation of Electronic Systems*, 3(3), pp. 496-514, July 1998.

[J2] H. Zhou and D. F. Wong. Global Routing with Crosstalk Constraints. *IEEE Transactions on Computer-Aided Design,* 18(11), pp. 1683-1688, November, 1999.

[J3] H. Zhou, D. F. Wong, I-M. Liu, and A. Aziz. Simultaneous Routing and Buffer Insertion with Restrictions on Buffer Locations. *IEEE Transactions on Computer-Aided Design*, 19(7), pp. 819-824, July, 2000.

[J4] H. Zhou and A. Aziz. Buffer Minimization in Pass Transistor Logic. *IEEE Transactions on Computer-Aided Design*, 20(5), pp. 693-697, May 2001.

[J5] H. Zhou, N. Shenoy, and W. Nicholls. Efficient Minimum Spanning Tree Construction without Delaunay Triangulation. *Information Processing Letters*, 81(5), pp. 271-276, 2002.

[J6] A. Goel, K. Sajid, H. Zhou, A. Aziz, and V. Singhal. BDD-based Procedures for a Theory of Equality with Uninterpreted Functions. *Journal of Formal Methods in System Design*, 22(3), pp. 205-224, May 2003.

[J7] H. Zhou. Timing Analysis with Crosstalk is a Fixpoint on a Complete Lattice. *IEEE Transactions on Computer-Aided Design*, 22(9), pp. 1261-1269, Sept. 2003. (**IEEE Donald O. Pederson Award finalist**)

[J8] H. Zhou. Efficient Steiner Tree Construction Based on Spanning Graphs. *IEEE Transactions on Computer-Aided Design*, 23(5), pp. 704-710, May 2004.

[J9] H. Zhou and C. Lin, Retiming for Wire Pipelining in System-On-Chip. *IEEE Transactions on Computer-Aided Design*, 23(9), pp. 1338-1345, Sept. 2004.

[J10] Q. Zhu, H. Zhou, T. Jing, X. Hong, and Y. Yang, Spanning Graph Based Non-Rectilinear Steiner Tree Algorithms. *IEEE Transactions on Computer-Aided Design*. 24(7), pp. 1066-1075, July 2005.

[J11] C. Lin and H. Zhou, Wire Retiming as Fixpoint Computation. *IEEE Transactions on VLSI Systems*. 13(12), pp. 1340-1348, Dec. 2005.

[J12] D. Sinha and H. Zhou, Gate-Size Optimization under Timing Constraints for Coupling-Noise Reduction. *IEEE Transactions on Computer-Aided Design*. 25(6), pp. 1064-1074, June 2006.

[J13] R. Chen and H. Zhou, Statistical Timing Verification for Transparently Latched Circuits. *IEEE Transactions on Computer-Aided Design*. 25(9), Sept. 2006.

[J14] C. Lin and H. Zhou, Optimal Wire Retiming Without Binary Search. *IEEE Transactions on Computer-Aided Design*. 25(9), Sept. 2006.

[J15] D. Sinha, N. Shenoy, and H. Zhou, Statistical Timing Yield Optimization by Gate Sizing. *IEEE Transactions on VLSI Systems*. 14(10), Oct. 2006.

[J16] R. Chen and H. Zhou, An Efficient Data Structure for Max-Plus Merge in Dynamic Programming. *IEEE Transactions on Computer-Aided Design*. 25(12), Dec. 2006.

[J17] D. Sinha and H. Zhou, Statistical timing analysis with coupling. *IEEE Transactions on Computer-Aided-Design*. 25(12), Dec. 2006.

[J18] A. Mallik, D. Sinha, P. Banerjee, and H. Zhou. Low Power Optimization by Smart Bit-Width Allocation in a SystemC Based ASIC Design Environment. *IEEE Transactions on Computer-Aided Design*. 26(3), pp. 447-455, Mar. 2007.

[J19] C. Lin and H. Zhou. Trade-off Between Latch and Flop for Min-Period Sequential Circuit Designs with Crosstalk. *IEEE Transactions on Computer-Aided Design*. 26(7), Jul. 2007.

[J20] C. Lin, J. Wang, and H. Zhou. Clustering for Processing Rate Optimization. *IEEE Transactions on VLSI Systems*. 26(8), Aug. 2007.

[J21] J. Wang and H. Zhou. Optimal Jumper Insertion for Antenna Avoidance under Ratio Bound. *IEEE Transactions on Computer-Aided Design*. 26(8), Aug. 2007.

[J22] D. Sinha, H. Zhou, and N. Shenoy. Advances in Computation of the Maximum of a Set of Gaussian Random Variables. *IEEE Transactions on Computer-Aided Design*. 26(8), Aug. 2007.

[J23] Z. Gu, J. Wang, R. Dick, and H. Zhou. Unified Incremental Physical-Level and High-Level Synthesis. *IEEE Transactions on Computer-Aided Design*. 26(9), Sep. 2007.

[J24] R. Chen and H. Zhou. An Efficient Algorithm for Buffer Insertion in General Circuits Based on Network Flow. *IEEE Transactions on Computer-Aided Design*. 26(11), Nov. 2007.

[J25] H. Zhou. A New Efficient Retiming Algorithm Derived by Formal Manipulation. *ACM Transactions on Design Automation of Electronic Systems*. 13(1). Article No. 7. Jan. 2008.

[J26] C.-W. Sham, F. Y. Young, and H. Zhou. Optimizing wirelength and routability by searching alternative packings in floorplanning. *ACM Tranactions Design Automation of Electronic Systems*. 13(1), Jan. 2008.

[J27] R. Chen and H. Zhou. Fast Estimation of Timing Yield Bounds for Process Variations. *IEEE Transactions on VLSI Systems*. 16(3), pp. 241-248, Mar. 2008.

[J28] J. Long, H. Zhou, and S. Ogrenci Memik. EBOARST: An Efficient Edge-Based Obstacle-Avoiding Rectilinear Steiner Tree Construction Algorithm. *IEEE Transactions on Computer-Aided Design*. Accepted for Publication, 2008.

Refereed Conference Proceedings

[C1] H. Zhou and D. F. Wong. An Optimal Algorithm for River Routing with Crosstalk Constraints. In *IEEE/ACM International Conference on Computer Aided Design*, San Jose, CA, November 1996.

[C2] C.-P. Chen, H. Zhou, and D. F. Wong. Optimal Non-uniform Wire-sizing under the Elmore Delay Model. In *IEEE/ACM International Conference on Computer Aided Design*, San Jose, CA, November 1996.

[C3] H. Zhou and D. F. Wong. An Exact Gate Decomposition Algorithm for Low-power Technology Mapping. In *IEEE/ACM International Conference on Computer Aided Design*, San Jose, CA, November 1997.

[C4] H. Zhou and D. F. Wong. Crosstalk Constrained Maze Routing Based on Lagrangian Relaxation. In *IEEE International Conference on Computer Design*, Austin, TX, October 1997.

[C5] H. Zhou and D. F. Wong. Global Routing with Crosstalk Constraints. In *ACM/IEEE Design Automation Conference*, San Francisco, CA, June 1998.

[C6] A. Goel, K. Sajid, H. Zhou, A. Aziz, and V. Singhal. BDD Based Procedures for a Theory of Equality with Uninterpreted Functions. In *International Conference on Computer Aided Verification*, Vancouver, British Columbia, June 1998.

[C7] H. Zhou, V. Singhal, and A. Aziz. How Powerful is Retiming? In *International Workshop on Logic Synthesis*, Lake Tahoe, CA, May 1998.

[C8] I.-M. Liu, T.-H. Liu, H. Zhou, and A. Aziz. Simultaneous PTL Buffer Insertion and Sizing for Minimizing Elmore Delay. In *International Workshop on Logic Synthesis*, Lake Tahoe, CA, May 1998.

[C9] H. Zhou, D. F. Wong, I-M. Liu, and A. Aziz. Simultaneous Routing and Buffer Insertion with Restrictions on Buffer Locations. In *ACM/IEEE Design Automation Conference*, New Orleans, LA, June 1999.

[C10] I-M. Liu, A. Aziz, D. F. Wong, and H. Zhou. An Efficient Buffer Insertion Algorithm for Large Networks Based on Lagrangian Relaxation. In *IEEE International Conference on Computer Design*, Austin, TX, October 1999.

[C11] H.-M. Chen, H. Zhou, F. Y. Young, D. F. Wong, H. H. Yang, and N. Sherwani. Integrated Floorplanning and Interconnect Planning. In *IEEE/ACM International Conference on Computer Aided Design*, San Jose, CA, November 1999.

[C12] H. Zhou and A. Aziz. Buffer Minimization in Pass Transistor Logic. In *ACM International Symposium on Physical Design*, San Diego, CA, April 2000.

[C13] H. Zhou and D. F. Wong. Optimal Low Power XOR Gate Decomposition. In *ACM/IEEE Design Automation Conference*, Los Angeles, CA, June 2000.

[C14] H. Zhou, N. Shenoy, and W. Nicholls. Efficient Minimum Spanning Tree Construction without Delaunay Triangulation. In *Asian and South Pacific Design Automation Conference*, Yokohama, Japan, January 2001.

[C15] H. Zhou, N. Shenoy, and W. Nicholls. Timing Analysis with Crosstalk as Fixpoints on Complete Lattice. In *ACM/IEEE Design Automation Conference*, Las Vegas, NV, June 2001.

[C16] S. H. Batterywala, N. Shenoy, W. Nicholls, and H. Zhou. Track Assignment: A Desirable Intermediate Step Between Global Routing and Detailed Routing. In *IEEE/ACM International Conference on Computer Aided Design*, San Jose, CA, 2002.

[C17] H. Zhou. Clock Schedule Verification with Crosstalk. In *Tau '02: ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, Monterey, CA, 2002.

[C18] C. W. Sham, F. Y. Young, and H. Zhou. Interconnect-Driven Floorplanning by Searching Alternative Packings. In *Asia and South Pacific Design Automation Conference*, Kitakyushu, Japan, 2003.

[C19] H. Zhou. Timing Verification with Crosstalk for Transparently Latched Circuits. In *DATE '03: Design Automation & Test in Europe*, Munich, Germany, 2003.

[C20] H. Zhou. Efficient Steiner Tree Construction Based on Spanning Graphs. In *ACM International Symposium on Physical Design*, Monterey, CA, 2003.

[C21] C. Lin and H. Zhou. Retiming for Wire Pipelining in System-On-Chip. In *IEEE/ACM International Conference on Computer Aided Design*, San Jose, CA, 2003. (**Best paper award nominee**)

[C22] Q. Zhu, H. Zhou, T. Jing, X. Hong, Y. Yang, Efficient Octilinear Steiner Tree Construction Based on Spanning Graphs. In *Asia and South Pacific Design Automation Conference*, Yokohama, Japan, 2004.

[C23] C. Lin and H. Zhou, Wire Retiming for System-On-Chip by Fixpoint Computation. In *DATE '04: Design Automation & Test in Europe*, Paris, France, 2004.

[C24] D. Sinha, H. Zhou, C.C.N. Chu, Optimal Gate Sizing for Coupling-Noise Reduction. In *ACM International Symposium on Physical Design*, Phoenix, AZ, 2004.

[C25] J. Wang and H. Zhou, Minimal Period Retiming under Process Variations. In *ACM Great Lakes Symposium on VLSI*, Boston, MA, 2004.

[C26] H. Zhou, A New Efficient Retiming Algorithm Derived by Formal Manipulation. In *International Workshop on Logic Synthesis*, Temecula, CA, 2004.

[C27] R. Chen and H. Zhou, A Flexible Data Structure for Efficient Buffer Insertion. In *IEEE International Conference on Computer Design*, San Jose, CA, 2004.

[C28] H. Zhou and J. Wang, ACG–Adjacent Constraint Graph for General Floorplans. In *IEEE International Conference on Computer Design*, San Jose, CA, 2004.

[C29] R. Chen and H. Zhou, Clock Schedule Verification Under Process Variations. In *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, 2004.

[C30] R. Chen and H. Zhou, Timing Macromodeling of IP Blocks with Crosstalk. In *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, 2004.

[C31] C. Lin and H. Zhou, Optimal Wire Retiming Without Binary Search. In *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, 2004.

[C32] D. Sinha and H. Zhou, Gate Sizing for Crosstalk Reduction under Timing Constraints by Lagrangian Relaxation. In *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, 2004.

[C33] D. Sinha and H. Zhou, Yield Driven Gate Sizing for Coupling-Noise Reduction under Uncertainty. In *Asia and South Pacific Design Automation Conference*, Shanghai, China, 2005.

[C34] J. Wang and H. Zhou, Interconnect Estimation Without Packing via ACG Floorplans. In *Asia and South Pacific Design Automation Conference*, Shanghai, China, 2005.

[C35] H. Zhou, Deriving a New Efficient Algorithm for Min-Period Retiming. In *Asia and South Pacific Design Automation Conference*, Shanghai, China, 2005.

[C36] M. Pan, C. C.-N. Chu and H. Zhou, Timing Yield Estimation Using Statistical Static Timing Analysis. In *IEEE International Symposium on Circuits and Systems*, Kobe, Japan, 2005.

[C37] X. Tang, H. Zhou, and P. Banerjee, Leakage Power Optimization with Dual-Vth Library in High-Level Synthesis. In *ACM/IEEE Design Automation Conference*, Anaheim, CA, 2005.

[C38] Z. Gu, J. Wang, R. P. Dick, and H. Zhou, Incremental Exploration of the Combined Physical and Behavioral Design Space. In *ACM/IEEE Design Automation Conference*, Anaheim, CA, 2005.

[C39] R. Chen and H. Zhou, Efficient Algorithms for Buffer Insertion in General Circuits Based on Network Flow. In *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, 2005.

[C40] C. Lin, J. Wang, and H. Zhou, Clustering for Processing Rate Optimization. In *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, 2005.

[C41] C. Lin and H. Zhou, Trade-off Between Latch and Flop for Min-Period Sequential Circuit Designs with Crosstalk. In *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, 2005.

[C42] D. Sinha, N. V. Shenoy, and H. Zhou, Statistical Gate Sizing for Timing Yield Optimization. In *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, 2005.

[C43] D. Sinha and H. Zhou, A Unified Framework for Statistical Timing Analysis with Coupling and Multiple Input Switching. In *IEEE/ACM International Conference on Computer Aided Design*, San Jose, CA, 2005.

[C44] N. Liveris, H. Zhou, and P. Banerjee, An Efficient System-Level to RTL Verification Framework for Computation-Intensive Applications. In *IEEE Asian Test Symposium*, Kolkata, India, 2005.

[C45] A. Mallik, D. Sinha, P. Banerjee, and H. Zhou, Smart Bit-Width Allocation for Low Power Optimization in a SystemC Based ASIC Design Environment. In *DATE '06: Design Automation and Test in Europe*, Munich, Germany, 2006.

[C46] D. Sinha, H. Zhou, and N. Shenoy, Advances in Computation of the Maximum of a Set of Random Variables. In *International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, 2006.

[C47] J. Wang, P. Wu, and H. Zhou, Processing Rate Optimization by Sequential System Floorplanning. In *International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, 2006.

[C48] C. Lin and H. Zhou, An Efficient Retiming Algorithm Under Setup and Hold Constraints. In *ACM/IEEE Design Automation Conference*, San Francisco, CA, 2006.

[C49] J. Wang and H. Zhou, Optimal Jumper Insertion for Antenna Avoidance under Ratio Upper-Bound. In *ACM/IEEE Design Automation Conference*, San Francisco, CA, 2006.

[C50] D. Das, A. Shebaita, H. Zhou, Y. Ismail, and K. Killpack. FA-STAC: A Framework for Fast and Accurate Static Timing Analysis with Coupling. In *IEEE International Conference on Computer Design*, San Jose, CA, 2006.

[C51] D. Sinha, D. Khalil, Y. Ismail, and H. Zhou, A Timing Dependent Power Estimation Framework Considering Coupling. *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, 2006.

[C52] C. Lin, H. Zhou, and C. Chu, A Revisit to Floorplan Optimization by Lagrangian Relaxation. In *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, 2006. (**Best paper award nominee**)

[C53] P. Narayana, R. Chen, Y. Zhao, Y. Chen, Z. Fu, and H. Zhou. Automatic Vulnerability Checking of IEEE 802.16 WiMAX Protocols through TLA+. In *Second Workshop on Secure Network Protocols*, Santa Barbara, CA, 2006.

[C54] S. Ozdemir, D. Sinha, G. Memik, J. Adams, H. Zhou. Yield-Aware Cache Architectures. In *MICRO-39: IEEE/ACM International Symposium on Microarchitecture*, Orlando, FL, 2006.

[C55] R. Chen and H. Zhou. Fast Buffer Insertion for Yield Optimization under Process Variations. In *ACM Asia South-Pacific Design Automation Conference*, Yokohama, Japan, 2007.

[C56] R. Chen and H. Zhou. New Block-based Statistical Timing Analysis Approaches without Moment Matching. In *ACM Asia South-Pacific Design Automation Conference*, Yokohama, Japan, 2007.

[C57] N. Liveris, C. Lin, J. Wang, H. Zhou, and P. Banerjee. Retiming for Synchronous Data Flow Graphs. In *ACM Asia South-Pacific Design Automation Conference*, Yokohama, Japan, 2007.

[C58] C. Lin and H. Zhou. Clock Skew Scheduling with Delay Padding for Prescribed Skew Domains. In *ACM Asia South-Pacific Design Automation Conference*, Yokohama, Japan, 2007.

[C59] D. Sinha, J. Luo, S. Rajagopalan, S. Batterywala, N. Shenoy and H. Zhou. Impact of Modern Process Technologies on the Electrical Parameters of Interconnects. In *International conference on VLSI Design and Embedded Systems*, Bangalore, India, 2007.

[C60] C. Lin, A. Xie, H. Zhou. Design Closure Driven Delay Relaxation Based on Convex Cost Network Flow. In *DATE: Design, Automation, and Test in Europe*, Nice, France, 2007.

[C61] R. Chen and H. Zhou. Fast Min-Cost Buffer Insertion Under Process Variations. ACM/IEEE Design Automation Conference, San Diego, CA, 2007.

[C62] J. Wang, D. Das, and H. Zhou. Gate Sizing by Lagrangian Relaxation Revisited. IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, 2007.

[C63] P. Zhou, Y. Ma, Z. Li, R. Dick, L. Shang, H. Zhou, X. Hong, and Q. Zhou. 3D-STAF: Scalable Temperature and Leakage Aware Floorplanning for Three-Dimentional Integrated Circuits. IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, 2007.

[C64] R. Chen and H. Zhou. Timing Budgeting Under Arbitrary Process Variations. IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, 2007.

[C65] N. Liveris, H. Zhou, and P. Banerjee. A Dynamic-Programming Algorithm for Reducing the Energy Consumption of Pipelined System-Level Streaming Applications. ACM Asia and South Pacific Design Automation Conference, Seoul, Korea, 2008.

[C66] D. Das, K. Killpack, C. Kashyap, A. Jas, and H. Zhou. Pessimism Reduction in Coupling Aware Static Timing Analysis Using Timing and Logic Filtering. ACM Asia and South Pacific Design Automation Conference, Seoul, Korea, 2008. (**Best paper award nominee**)

[C67] J. Long, H. Zhou, and S. Ogrenci Memik. An $O(n \log n)$ Edge-Based Algorithm for Obstacle-Avoiding Rectilinear Steiner Tree Construction. ACM International Symposium on Physical Design, Portland, OR, 2008.

[C68] J. Wang and H. Zhou. An Efficient Incremental Algorithm for Min-Area Retiming. ACM/IEEE Design Automation Conference, Anaheim, CA, 2008.

[C69] N. Liveris and H. Zhou. Retiming and Resynthesis with Sweep is Complete for Sequential Transformations. International Workshop on Logic and Synthesis, Lake Tahoe, CA, 2008.

[C70] N. Liveris, H. Zhou, R. Dick, and P. Banerjee. State Space Abstraction for Parameterized Self-Stabilizing Embedded Systems. International Conference on Embedded Software (EMSOFT), Atlanta, GA, 2008.

[C71] J. Wang and H. Zhou. Linear Constraint Graph for Floorplan Optimization with Soft Blocks. IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, 2008.

Selected Invited Lectures

[L1] "Efficient Incremental Algorithms for Retiming" invited talk, University of Colorado, Boulder, CO, February 2008.

[L2] "Floorplan Representation and Optimization," invited talk, National Jiao Tung University, Taiwan, August 2007.

[L3] "Optimization Algorithm Design in VLSI CAD," invited talk, National Taiwan University, National Tsing Hua University, Taiwan, August 2007.

[L4] "Optimization Techniques For System-on-Chip," invited tutorial, 18th VLSI Design and CAD Symposium, Hualien, Taiwan, August 2007.

[L5] "Advanced Algorithm Design in VLSI CAD," invited short course, Tsinghua University, Beijing, China, July 2006.

[L6] "To Optimize or Not to Optimize: Algorithm Design in VLSI CAD," invited lecture, *Meet the EECS Faculty Seminar*, Northwestern University, May 2006.

[L7] "To Optimize or Not to Optimize: Algorithm Design in VLSI CAD," invited lecture, *ECE Distinguished Speaker Seminar Series*, Illinois Institute of Technology, April 2006.

[L8] "Efficient Retiming Algorithms for Wire Pipelining in System-on-Chip," invited lecture, University of California at Berkeley, November 2005.

[L9] "Efficient Retiming Algorithms for Wire Pipelining in System-on-Chip," invited lecture, University of Illinois at Chicago, June 2005.

[L10] "Efficient Retiming Algorithms for Wire Pipelining in System-on-Chip," invited lecture, University of Michigan, Ann Arbor, MI, May 2005.

[L11] "Interconnection vs. Packing: Modern Floorplanning via ACG," invited lecture, Synopsys, Mountain View, CA, November 2004.

[L12] "Interconnection vs. Packing: Modern Floorplanning via ACG," invited lecture, Cadence Design Systems, San Jose, CA, October 2004.

[L13] "VLSI CAD Research in NU: Timing Verification in Deep Sub-Micron," invited lecture, Motorola, Arlington Heights, IL, April 2003.

[L14] "CAD Research in Northwestern University," invited lecture, Tsinghua University, Beijing, China, December 2002.

[L15] "Efficient Routing Tree Algorithms," invited lecture, Xilinx, San Jose, CA, November 2002.

[L16] "Timing Verification in Presence of Crosstalk," invited lecture, Cadence Design Systems, San Jose, CA, November 2002.

[L17] "Timing Verification and Optimization," invited lecture, Intel Corp, Hillsboro, OR, August 2002.

[L18] "Circuit Semantics: Timing Analysis with Crosstalk," invited lecture, Avanti Corp, Fremont, CA, January 2002.

[L19] "Methodology and Tools for Modern Hardware Design," invited lecture, Northwestern University Technology Update, December 2001.

[L20] "Restore Semantics to Circuits: Modeling Timing with Crosstalk as a Fixpoint," invited lecture, Synopsys, Mountain View, CA, July 2001.

Theses Supervised

[T1] Jia Wang, "System-Level Optimizations for High Performance DSM Circuits," Ph.D. Dissertation, Northwestern University, June 2008. (EECS Best Dissertation, currently with Illinois Institute of Technology).

[T2] Ruiming Chen, "Timing Analysis and Optimization Techniques for VLSI Circuits," Ph.D. Dissertation, Northwestern University, December 2007. (currently with Synopsys)

[T3] Chuan Lin, "Timing Optimization Algorithms for Sequential Circuits," Ph.D. Dissertation, Northwestern University, June 2006. (currently with Magma Design Automation)

[T4] Debjit Sinha, "Analysis and Optimization under Crosstalk and Variability in Deep Sub-Micron VLSI Circuits," Ph.D. Dissertation, Northwestern University, June 2006. (currently with IBM)

[T5] Jia Wang, "Adjacent Constraint Graph and Its Applications," M.S. Thesis, Northwestern University, June 2005. (going on for Ph.D. in Northwestern)

Thesis Committees Served on

[G1] M. Haldar, "Optimized Hardware Synthesis for FPGAs," (supervised by P. Banerjee and A. Choudhary) Ph.D. Dissertation, Northwestern University, August 2001.

[G2] A. Nayak, "Automatic Parallelization and Optimizations for Synthesizing MATLAB Programs on Multi-FPGA Systems," (supervised by P. Banerjee and A. Choudhary) Ph.D. Dissertation, Northwestern University, August 2001.

[G3] A. Jones, "PACT HDL: A C Compiler Targeting ASICs and FPGAs with Power and Performance Optimizations," (supervised by P. Banerjee) Ph.D. Dissertation, Northwestern University, August 2002.

[G4] J. Pramod, "A Type Inference System for MATLAB with Applications to Code Optimization," (supervised by P. Banerjee) Ph.D. Dissertation, Northwestern University, August 2003.

[G5] R. Mukherjee, "System Level Synthesis of IP Blocks in the PACT Compiler" (supervised by P. Banerjee) M.S. Thesis, Northwestern University, June 2003.

[G6] N. Liveris, "Power Aware Interface Synthesis for Bus-Based SOC Design" (supervised by P. Banerjee) M.S. Thesis, Northwestern University, June 2003.

[G7] A. Mallik, "An Algorithm for Low Power Optimization with Quantization Error Constraints in SystemC based ASIC Design" (supervised by P. Banerjee) M.S. Thesis, Northwestern University, June 2004.

[G8] S. Mei, "Frequency Dependent VLSI Circuit Modeling and Design" (supervised by Y. Ismail) Ph.D. Dissertation, Northwestern University, June 2004.

[G9] X. Tang, "High-Level Synthesis Algorithms for Low Power ASIC Design," (supervised by P. Banerjee) Ph.D. Dissertation, Northwestern University, June 2004.

[G10] T. Jiang, "Power Aware High-level Synthesis Techniques for FPGAs," (supervised by P. Banerjee) Ph.D. Dissertation, Northwestern University, June 2004.

[G11] G. Mittal, "Compiler Infrastructure for Compiling Assembly and Binary Programs onto Field Programmable Gate Arrays," (supervised by P. Banerjee) Ph.D. Dissertation, Northwestern University, August 2004.

[G12] C. Amin, "Timing Analysis of High Performance Integrated Circuits" (supervised by Y. Ismail) Ph.D. Dissertation, Northwestern University, June 2005.

[G13] D. Zaretsky, "A Methodology for Mapping Scheduled Software Binaries onto Field Programmable Gate Arrays," (supervised by P. Banerjee) Ph.D. Dissertation, Northwestern University, December 2005.

[G14] M. Ghoneima, "Improving the Bit-Rate, Noise Performance and Power Dissipation of On-Chip Buses" (supervised by Y. Ismail) Ph.D. Dissertation, Northwestern University, June 2006.

[G15] D. Jariwala, "Mechanisms for Tighter Integration of Placement and Routing" (supervised by J. Lillis) Ph.D. Dissertation, University of Illinois, Chicago, August 2006.

Current Students

- Bach Ha (Ph.D., expected 6/11)
- Nikos Liveris (Ph.D., co-supervised with P. Banerjee, expected 6/08)
- Debasish Das (Ph.D., expected 6/09)

Northwestern University Committees and Service

- Chair, ECE Distinguished Seminar Committee, 2002-2005.
- EECS Distinguished Seminar Committee, 2006-present.
- ECE Teaching and Awards Committee, 2001-present.
- Computer Engineering Curriculum Committee, 2001-present.
- Computational Biology and Bioinformatics Program Curriculum Committee, 2004-present.
- ECE Department Search Committee (Computer Engineering area) 2002-2004.
- EECS Department Search Committee (Theoretical Computer Science area), 2006.
- Organizer, ECE department "Mathematics/Algorithms Discussion (MAD) Series," 2001-present.