

Lab 4 Finite State Machine Design and Simulation

In this lab, you will use Mentor Graphics tools to design a sequential circuit (also known as a finite state machine) and simulate it. You are assumed familiar with the tools through labs 1 and 2.

The machine you need to design is described as follows.

A finite state machine has one input (X) and two outputs (Z_1 and Z_2). An output $Z_1 = 1$ occurs every time the input sequence 101 is observed, provided the sequence 011 has never been seen. An output $Z_2 = 1$ occurs every time the input 011 is observed. Note that once $Z_2 = 1$, $Z_1 = 1$ can never occur. You need to implement the machine in the Mealy design style.

First, you need to work out the symbolic state diagram by pencil and paper. If you have more than eight states, try to reduce the state number by state minimization. Second, do a state assignment by hand (do your best to simplify the design). Assuming D flip-flops are used, you then need to generate the next state functions and output functions. Finally, we need to input your design to Mentor Graphics tools and do simulations on it.

When constructing the schematics in Mentor Graphics, you can find the D flip-flops and other gates in the library (as you have done in lab 2). Then you need to set up the clock signal and the input sequence for simulation (which you should be able to do based on your experience in lab 2). Be careful with the synchronization of inputs and the clock. You may simulate any input sequences you want, but please include the following input sequence:

111001010001101011

You need to turn in your symbolic state diagram, state transition table after the state assignment, the next state and output functions, the schematics of the design, and the simulation wave forms.