ECE357: Introduction to VLSI CAD

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Fall 2001

Logistics

- Time & Location: MWF 11-11:50 TECH LG68
- Instructor: Hai Zhou `haizhou@ece.nwu.edu`
- Office: L461
- Office Hours: MW 3-4P
- Teaching Assistant: TBA
- Reference Texts:
  VLSI Physical Design Automation: Theory & Practice, Sait & Youssef, World Scientific, 1999.
  An Introduction to VLSI Physical Design, Sarrafzadeh & Wong, McGraw Hill, 1996.

- Grading: Project-40% Midterm-30% Homework-30%
- Homework must be turned in before class on each due date, late: -40% per day
- Course homepage: `www.ece.nwu.edu/~haizhou/ece357.html` Please check it frequently for updates.

What can you expect from the course

- Understand modern VLSI design flows (but not the details of tools)
- Understand the physical design problem
- Familiar with the stages and basic algorithms in physical design
- Improve your capability to design algorithms to solve problems
- Improve your capability to think and reason

What do I expect from you

- Active and critical participation
  - correct my omissions and mistakes
  - speed me up or slow me down if my pace mismatches yours
  - "Your role is not one of sponges, but one of whetstones; only then the spark of intellectual excitement can continue to jump over"
- Write as if your work is to be published
  - be careful with sentences, notations, and logic behind reasonings
- You can discuss homework with your classmates, but need to write down solutions independently

VLSI (Very Large Scale Integrated) chips

- VLSI chips are everywhere
  - computers
  - commercial electronics: TV sets, DVD, VCR, ...
  - voice and data communication networks
  - automobiles
- VLSI chips are artifacts
  - they are produced according to our will ...

Design: the most challenging human activity

- Design is a process of creating a structure to fulfill a requirement
- Strictly speaking, design is a human activity
- Brain power is the scarcest resource
  - Delegate as much as possible to computers–CAD
- Avoid two extreme views:
  - Everything manual: impossible–millions of gates
  - Everything computer: impossible either
- Very important to understand boundaries–methodology

Design is always difficult

A main task of a designer is to manage complexity

- Silicon complexity: physical effects no longer be ignored
  - resistive and cross-coupled interconnects; signal integrity; weak and faster gates
  - reliability; manufacturability
- System complexity: more functionality in less time
  - gap between design and fabrication capabilities
  - desire for system-on-chip (SOC)

Design challenges

- Silicon complexity requires design process to be more close to physical details
- System complexity requires design process to be more abstract to handle larger systems
- They stretch design process in opposite directions

CAD: A tale of two designs

- Target–hardware design
  - methodology
  - correctness
- Aid–software design (programming)
  - methodology
  - correctness
- Be conscious of their similarities and differences

Emphasis of the course

- Design methodology
  - a specific design problem may be simplified or eliminated if we use a different design method
- Algorithms
  - show your algorithm is correct and efficient
  - do not be scared by NP-hardness
- Be conscious and try to improve problem solving skills

Basics of hardware design

- Two enabling techniques
  - Boolean decomposition theorem
  - MOS FET device technology
- Most CAD techniques only concern about how to design and implement the structure of system, therefore are useful even basic devices are changed.

Boolean decomposition theorem

- Any n-input Boolean function $F : B^n \rightarrow B$ can be implemented as a connection of two-input Boolean functions.
- Both $\{\neg, \wedge\}$ and $\{\neg, \vee\}$ are complete for the above purpose.

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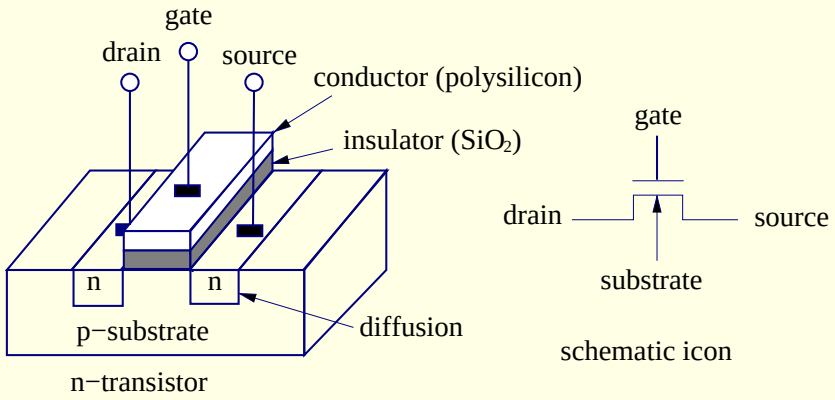
Please give a proof.

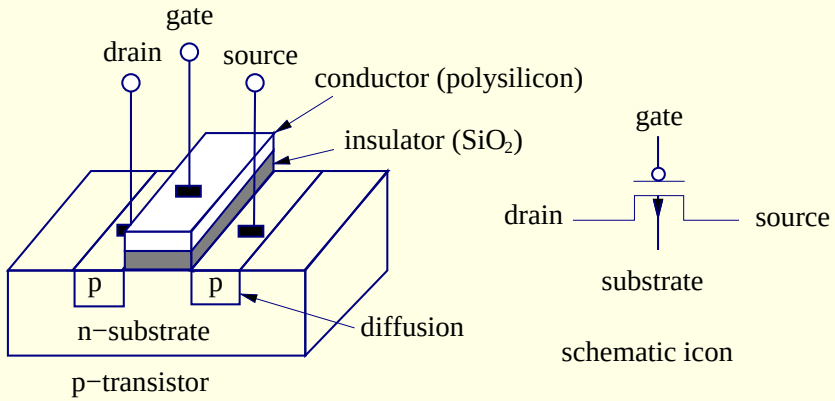
Basics of MOS Devices

- The most popular VLSI technology: MOS (Metal-Oxide-Semiconductor).
- CMOS (Complementary MOS) dominates nMOS and pMOS, due to CMOS's lower power dissipation, high regularity, etc.
- Physical structure of MOS transistors and their schematic icons: nMOS, pMOS.
- Layout of basic devices:
  - CMOS inverter
  - CMOS NAND gate
  - CMOS NOR gate

MOS Transistors

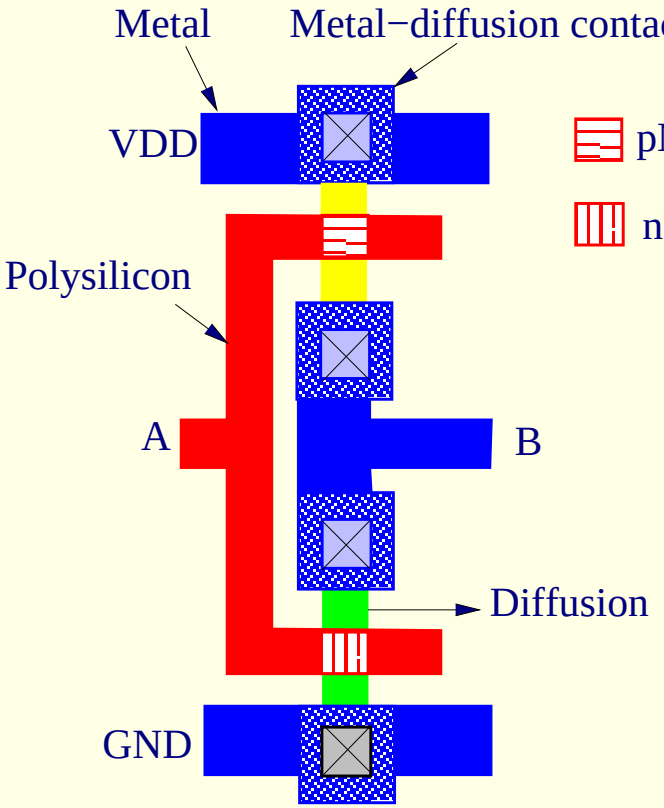


The nMOS switch passes "0" well.



The pMOS switch passes "1" well.

A CMOS Inverter

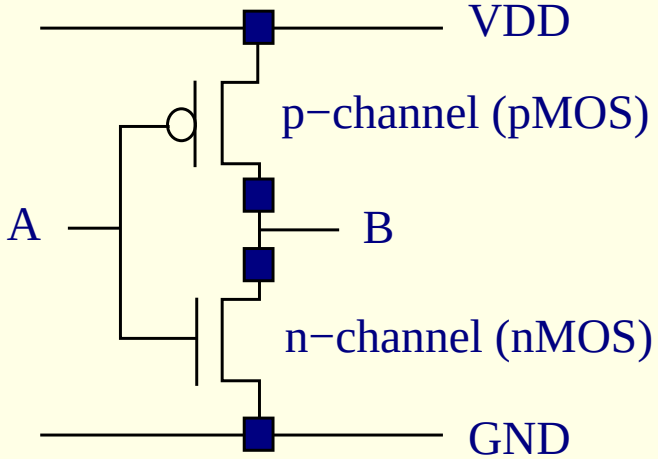


layout

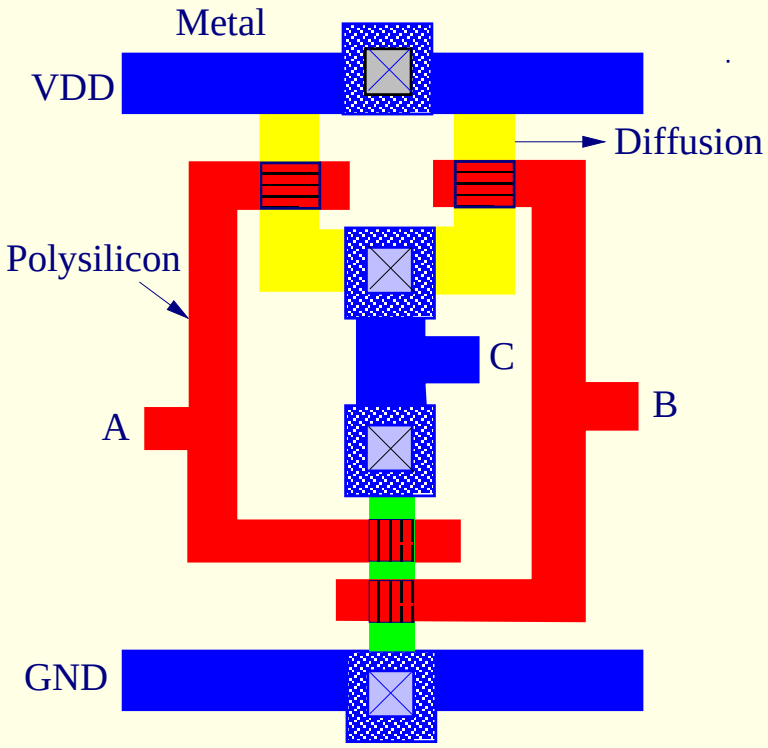
pMOS transistor

nMOS transistor

A	B
1	0
0	1

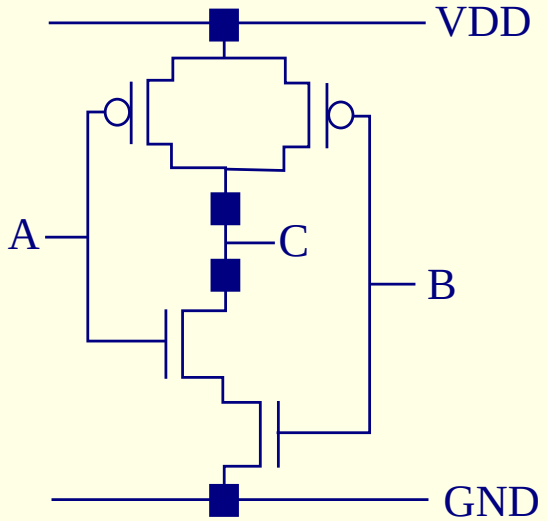


A CMOS NAND Gate

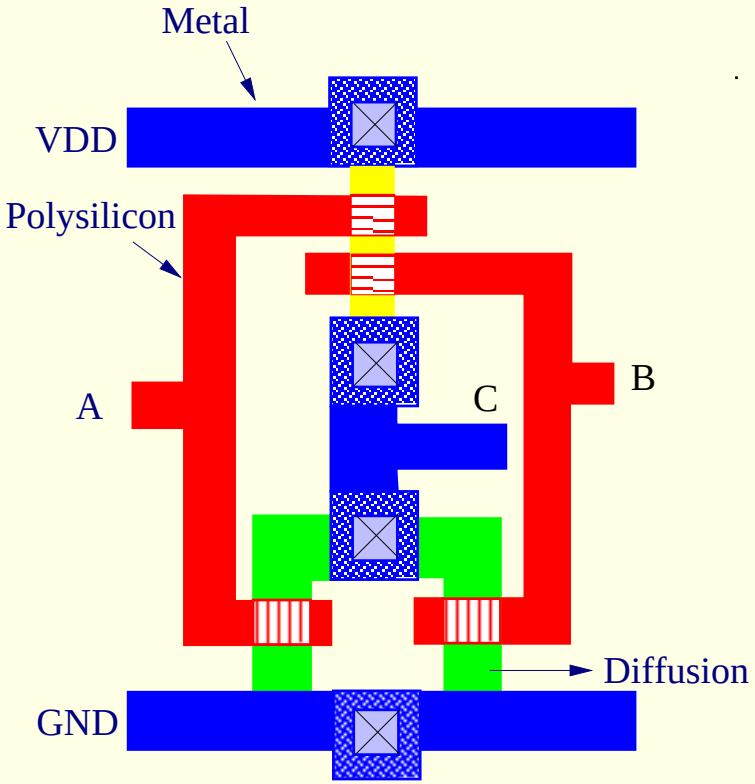


layout

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

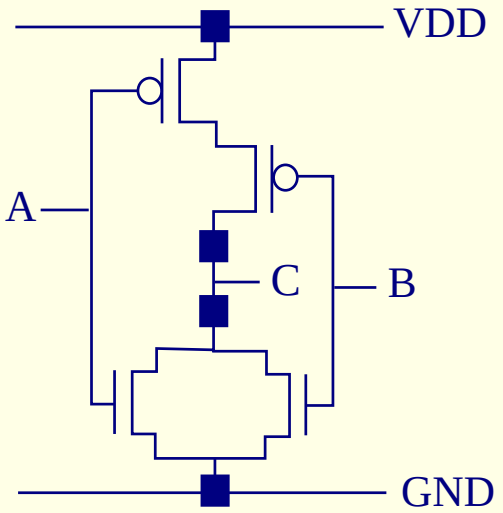


A CMOS NOR Gate



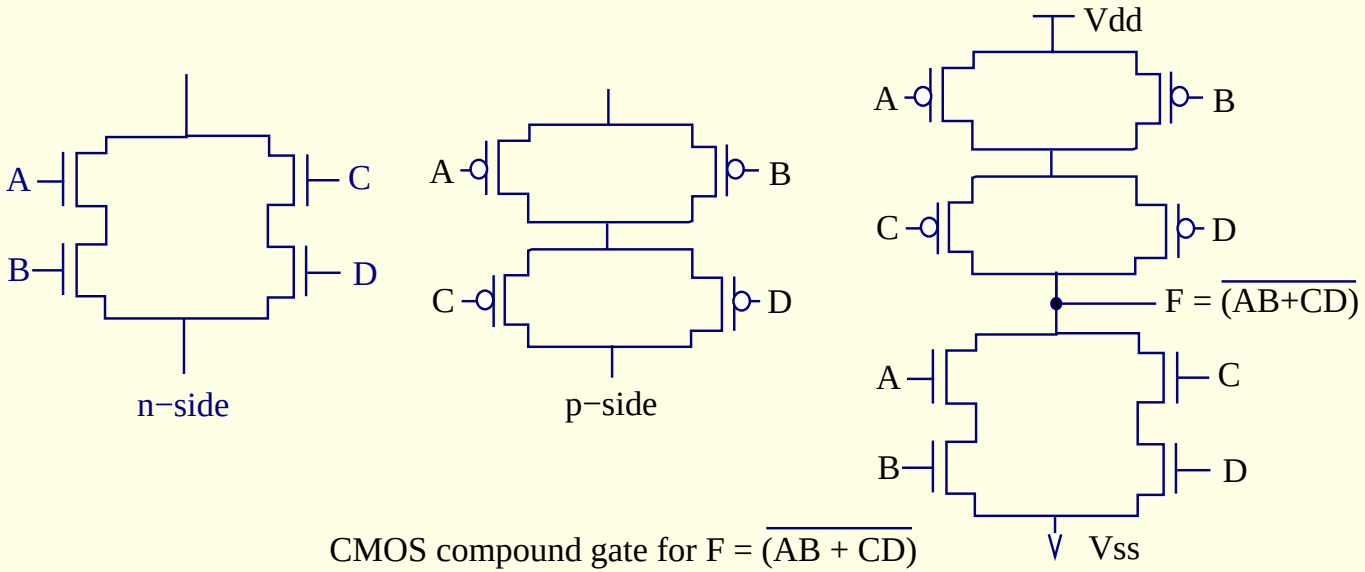
layout

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0



Construction of Compound Gates

- Example: $F = \overline{A \cdot B + C \cdot D}$.
- Step 1: Invert F to derive n-network ($\overline{F} = A \cdot B + C \cdot D$).
- Step 2: Make connections of transistors:
  - AND $\Longleftrightarrow$ Series connection; OR $\Longleftrightarrow$ Parallel connection.
- Step 3: Expand F to derive p-network ($F = \overline{AB + CD} = \overline{AB} \cdot \overline{CD} = (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})$); each input is inverted.
- Step 4: Make connections of transistors (same as Step 2).
- Step 5: Connect the n-network to GND (typically, 0V) and the p-network to VDD (5V, 3.3V, or 2.5V).



CMOS compound gate for F = $\overline{(AB + CD)}$