# Yield Driven Gate Sizing for Coupling-Noise Reduction under Uncertainty

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*Abstract*— **This paper presents a post-route gate-sizing algorithm for coupling-noise reduction that constrains the yield loss under process variations. Algorithms for coupling-noise reduction which do not consider uncertainty in the manufacturing process can make a circuit susceptible to failure. Using probabilistic models, the coupling-noise reduction problem is solved as a fixpoint computation problem on a lattice. A novel gate-sizing algorithm with low area overhead is proposed for coupling-noise reduction under uncertainty. Experimental results are reported for the ISCAS benchmarks and larger circuits with comparisons to traditional approaches.**

## I. Introduction

Shrinking geometries have led to a reduction in the self capacitance of wires in modern VLSI circuits. However, increased aspect ratio of the wires increase coupling capacitances between them. Coupling induces noise on the coupled nets, which can cause functionality failures in the circuit. For present day processes, the coupling capacitance can be as high as the sum of the area capacitance and the fringing capacitance. Trends indicate that the significance of coupling capacitances will be even more dominant in the future as feature sizes shrink [1]. This makes coupling-noise critical in IC design.

Coupling-noise induced on a net is dependent on the size of its driving-gate and the driving-gate size of each net coupled to it. Various design approaches try to minimize coupling-noise in early stages of design. It is necessary to ensure that the maximum noise induced on every net is bounded. The noise upper-bound requirement for every net in the circuit is called the noise-constraint. In the post-routing stage, coupling-noise on some nets may still be critical which need to be fixed. In this scenario, gate-sizing is an attractive approach to noise reduction since it may not require re-routing. Scalable libraries and existing fill space can be used for gate-sizing.

Coupling-noise induced on a net can be reduced if the size of its driving-gate is increased, or if driving-gate sizes of the coupled nets are decreased. However, when the driving-gate of a net is sized up, it may increase the noise it induces on other nets as an aggressor. On the other hand, when the driving-gate size of an aggressor is reduced, noise induced on itself may increase. Since coupling is symmetric on the coupled nets, it is artificial to classify nets as aggressors or victims. A net could be an aggressor and a victim at the same time. Though it is plausible to classify a net based on the strength of the noise on itself and other coupled nets, with changing driving-gate sizes, the role of a net may change. This motivates refraining from classification of nets as aggressors or victims in this paper.

As CMOS feature sizes move into the DSM regime, the effects of process variations become critical with the increase in the variability of process parameters [2]–[4]. Variances in parameters such as gate-length, dopant concentration and gate-thickness affect circuit performance. Design methodologies need to guarantee a minimal level of certainty in terms of circuit performance. Conventional methods take worst case values for design, but yield pessimistic results. Probabilistic approaches are now considered more appropriate.

Gate-sizing for coupling-noise reduction has been shown to be effective by researchers in the past. Xiao *et al.* [5] propose a transistor sizing algorithm for crosstalk reduction. They use the SNOPT NLP solver to solve the formulated problem. The gate-sizing algorithm for crosstalk-noise optimization which Hashimoto *et al.* [6] propose is limited to sizing down the driving-gates of aggressor nets only. Becer *et al.* [7] propose an algorithm which classifies nets as aggressors or victims and does not guarantee an optimal solution. Sinha *et al.* [8] propose an optimal gate-sizing algorithm for coupling-noise reduction. The optimal gate-sizing algorithm finds minimum gate-sizes under given physical and timing constraints such that nets satisfy given noise constraints. In [9], Sinha *et al.* propose another gate-sizing algorithm for crosstalk reduction, which is based on Lagrangian Relaxation. The above algorithms do not consider effects due to process variations. Variability affects coupling between nets, and can cause noise induced on a net to overshoot its required constraint. Yield in this paper denotes the probability that all nets of a circuit satisfy coupling-noise constraints. The desire to achieve a lower bound on the yield motivates the yield driven gate-sizing problem for coupling-noise reduction.

An iterative gate-sizing algorithm for coupling-noise reduction is proposed, which constrains the yield loss under process variations. The yield driven gate-sizing problem for noise reduction is translated into a fixpoint computation problem similar to [8] and [10]. A gate-sizing transformation is developed, the solutions to which are mapped onto a complete lattice. The effectiveness of the algorithm is validated by simulations on the ISCAS benchmarks [11] and three larger circuits. Results are compared with those from the optimal gate-sizing algorithm [8] and an alternative design approach which uses a guard-band during sizing to account for uncertainty.

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The rest of the paper is organized as follows. The yield driven gate-sizing problem for coupling-noise reduction is formulated in section II and the theoretical concepts of gate-sizing as a fixpoint computation are explained in section III. The iterative gate-sizing algorithm is presented in section IV and experimental results are reported in section V. Conclusions and future work are discussed in section VI.

## II. Problem Formulation

### A. Gate Sizes as Random Variables

Fabricated gate-sizes cannot be accurately predicted due to variations in the manufacturing process. Probabilistic models consider the uncertain parameters as random variables. Variabilities in parameters like gate-length, dopant concentration and gate-thickness cause the effective gate-resistance *(Rd)* to be a random variable, the distribution of which is assumed to be Gaussian [12]. The theory and concepts behind the proposed approach apply to other distributions as well. The driving-gate size of a net $i$ is denoted as a Gaussian random variable $s(i) = N(\mu_i, \sigma_i^2)$, having a mean value of $\mu_i$ and variance $\sigma_i^2$.

### B. Coupling Graph

An undirected *coupling-graph* is used to model a circuit and its coupling information. Nodes in the graph represent nets in the circuit. An edge in the graph represents significant coupling between nets corresponding to the two nodes it joins. Edges in the coupling-graph are called coupling-edges. In the extreme case an edge may be introduced between two nodes if their corresponding nets have any coupling.

### C. Problem definition

The syntax of single notation quantification is used for all mathematical relations and expressions in the paper. This is similar to the one advocated by Gries and Schneider [13]. The general form of a quantification over a binary operator $\star$ is exemplified by

$$(\star x : R : P)$$

where variable $x$ is called the *bound variable* or *dummy* of the quantification, $R$ is a boolean expression called the *range* of the quantification such that values assumed by $x$ satisfy $R$, and $P$ is an expression which is called the *body* of the quantification. The above expression denotes the application of the operator $\star$ to the values of $P$ for all $x$ for which range $R$ is $true$. For example, $\sum_{i=1}^{n} x_i$ would be represented as $(+i : 1 \leq i \leq n : x_i)$ and $\forall x\ R \rightarrow P$ as $(\forall x : R : P)$.

Given the size of all gates in a circuit, the noise induced on each net can be calculated using a noise-model. It is not necessary that the noise-model be an analytical one. Based on the coupling-graph model as introduced above and assuming gate-sizes have a normal distribution, the noise $\eta(i)$ on a given net $i$ can be represented as

$$\eta(i) \stackrel{\triangle}{=} f_i(N(\mu_i, \sigma_i^2), N(\mu_{i_1}, \sigma_{i_1}^2) \ldots N(\mu_{i_k}, \sigma_{i_k}^2))$$

or simply as

$$\eta(i) \stackrel{\triangle}{=} f_i(s(i), s(i_1), \ldots, s(i_k))$$

where $i_1, \ldots, i_k$ represents nets which couple to $i$, and $s(i_1), \ldots, s(i_k)$ represents their driving-gate sizes respectively. Nominal gate-sizes can be represented as a gate-size vector $M$ as following

$$M \stackrel{\triangle}{=} (i : 0 \leq i < n : \mu_i)$$

A circuit is considered to satisfy the noise constraint if coupling-noise $\eta(i)$ on every net $i$ is upper bounded by $U_i$. The nominal driving-gate size $\mu_i$ of a net $i$ is bounded by $l(i)$ and $u(i)$, which represent minimum and maximum bounds on the gate-size given by physical and timing constraints.

The objective of the optimal gate-sizing problem for noise reduction under uncertainty is to find the minimal gate-size vector $M$ such that a given lower bound on the yield can be guaranteed. This optimization problem is approached in two stages. Given that the desired yield for a design (henceforth referred as the *global yield*) is distributed into probabilities of no noise violation on each net (henceforth referred to as *local yield*), the yield driven gate-sizing problem attains to find optimal gate-sizes that achieve the local yields throughout the circuit. In the ideal case a global yield of $100\%$ could be distributed as desired local yields of $100\%$ throughout the circuit. This paper presents a method to achieve the desired yields in different parts of the circuit and finds optimal gate-sizes for the same under given physical and timing constraints. It presents an algorithm to solve the yield driven gate-sizing problem for coupling-noise reduction.

## III. Gate sizing as a fixpoint computation

### A. Obtaining a fixpoint of the Gate Sizing Transformation

Irrespective of the noise model being used, for any net $i$, the noise function $f_i(s(i), s(i_1), \ldots, s(i_k))$ is considered to be monotonically non-increasing on $s(i)$ and monotonically non-decreasing on $s(i_j)$ for any $1 \leq j \leq k$. This assumption is conservative and is satisfied by any reasonable noise-function. Similar assumptions based on evidence were used in [5]. The monotonic property is formally expressed as

$$s(i) < s'(i) \quad (1)$$
$$\Rightarrow \quad f_i(s(i), s(i_1), \ldots, s(i_k)) \geq f_i(s'(i), s(i_1), \ldots, s(i_k))$$

$$s(i_j) < s'(i_j) \quad (2)$$
$$\Rightarrow \quad f_i(s(i), \ldots, s(i_j), \ldots s(i_k)) \leq f_i(s(i), \ldots, s'(i_j), \ldots s(i_k))$$

Based on the monotonic property, $g_i$ is defined to be a function of driving-gate sizes of nets that couple to $i$. It gives the minimal driving-gate size of $i$ satisfying physical and timing constraints, such that the probability of the net being noise free under uncertainty is lower bounded by $Y_i$. The given bound for the minimum probability $Y_i$ is called the desired local yield of net $i$. Formally, $g_i$ is defined as

$$g_i(\mu_{i_1}, \mu_{i_2}, \ldots, \mu_{i_k}) \stackrel{\triangle}{=} \quad (3)$$

$$(min\ x: \quad (Pr(f_i(N(x,\sigma_i^2), s(i_1), \ldots, s(i_k)) \leq U_i)) \geq Y_i) \\ \wedge\ (l(i) \leq x \leq u(i)) : x)$$

where $Pr(k)$ denotes the probability of event $k$. A system of equations is thus formed when gate-sizes for all nets are combined:

$$(\ \forall i : 0 \leq i < n : \mu_i = g_i(\mu_{i_1}, \mu_{i_2}, \ldots, \mu_{i_k})\ )$$

If nominal gate-sizes and the transformations are represented as vectors $M = (i : 0 \leq i < n : \mu_i)$, and $G = (i : 0 \leq i < n : g_i)$, the above equation can be written as:

$$M = G(M) \tag{4}$$

A solution to (4) is a gate-size vector $M$, which is called a fixpoint of $G$. (4) is next shown to be a necessary condition for the solution to the yield driven gate-sizing problem.

*Theorem 1:* The solution to the yield driven gate-sizing problem lies within the solution space of (4)

*Proof:* Let $M'$ be the solution to the yield driven gate-sizing problem and $M'' = G^k(M')$ such that $G(M'') = M''$, for some $k > 0$. $G^k(M)$ represents successive applications of transformation $G$ on the vector $M$. Transformation $G^k$ on vector $M'$ that satisfies the yield and size constraints, gives vector $M''$ such that driving-gate size of every net in $M''$ is less than or equal to the same in $M'$. This is deduced from the definition of $g_i$ in (3), which ensures that a gate is never over-sized. Since the vector $M'$ satisfies the yield constraints, successive $G$ transformations will not increase the driver size of any net, and may only size them down. The above shown relation between the two gate-size vectors is expressed as $M'' \leq M'$.

$M'$ is the minimal vector of gate-sizes satisfying yield and size constraints. Since $M''$ also satisfies the yield and size constraints, and $M'' \leq M'$, it is evident that $M''$ and $M'$ are identical. Fixpoint $M''$ is therefore shown to be the solution to the yield driven gate sizing problem. ■

It is thus established that a solution to the yield driven gate-sizing problem is also a fixpoint of $G$. However, the converse is not true. An arbitrary fixpoint of $G$ may not be a minimal solution to the gate-sizing problem. A gate-size vector that satisfies (4) can be a solution to the original problem if and only if it yields the minimal gate-size vector among all other fixpoints of $G$. There arises a need to study the fixpoint of $G$ that is a solution to the gate-sizing problem and also the way to find it.

A partial order $\leq$ between vectors $X$ and $Y$ is defined as

$$(X \leq Y) \stackrel{\triangle}{=} (\forall i : 0 \leq i < n : x(i) \leq y(i))$$

*Theorem 2:* If $M_1 \leq M_2$, then $G(M_1) \leq G(M_2)$.

*Proof:* From the above definition, $M_1 \leq M_2$ implies that

$$(\forall i : 0 \leq i < n : \mu_{1_i} \leq \mu_{2_i}) \tag{5}$$

The theorem is proved using contradiction. If $G(M_1) \leq G(M_2)$ is not true, then

$$(\exists j : 0 \leq j < n : \\ g_j(\mu_{1_{j_1}}, \ldots, \mu_{1_{j_k}}) > g_j(\mu_{2_{j_1}}, \ldots, \mu_{2_{j_k}}) \tag{6}$$

Variables $m$ and $n$ are defined as

$$m \stackrel{\triangle}{=} g_j(\mu_{1_{j_1}}, \mu_{1_{j_2}}, \ldots, \mu_{1_{j_k}}) \\ n \stackrel{\triangle}{=} g_j(\mu_{2_{j_1}}, \mu_{2_{j_2}}, \ldots, \mu_{2_{j_k}})$$

(6) can now be expressed as

$$m > n \tag{7}$$

The following definitions are next considered

$$\eta_1 \stackrel{\triangle}{=} f_j(N(n,\sigma_j^2), s_1(j_1), s_1(j_2), \ldots, s_1(j_k)) \\ \eta_2 \stackrel{\triangle}{=} f_j(N(n,\sigma_j^2), s_2(j_1), s_2(j_2), \ldots, s_2(j_k))$$

Given the monotonic property of the noise function $f_j$ from (2), and nominal size relations from (5), it can be shown that

$$Pr(\eta_1 \leq U_j) \geq Pr(\eta_2 \leq U_j) \tag{8}$$

From the definitions of $n$ and $g_i$ in (3)

$$n = g_j(\mu_{2_{j_1}}, \mu_{2_{j_2}}, \ldots, \mu_{2_{j_k}}) \\ \Rightarrow \quad Pr(f_j(N(n,\sigma_j^2), s_2(j_1), s_2(j_2), \ldots, s_2(j_k)) \leq U_j) \geq Y_j \\ \Rightarrow \quad Pr(\eta_2 \leq U_j) \geq Y_j$$

Combining (8) and the one obtained above

$$(Pr(\eta_1 \leq U_j) \geq Pr(\eta_2 \leq U_j)) \wedge (Pr(\eta_2 \leq U_j) \geq Y_j) \\ \Rightarrow \quad Pr(\eta_1 \leq U_j) \geq Y_j \\ \Rightarrow \quad Pr(f_j(N(n,\sigma_j^2), s_1(j_1), s_1(j_2)\ldots) \leq U_j) \geq Y_j)$$

However, from the definitions of $m$ and $g_i$

$$m = g_j(\mu_{1_{j_1}}, \mu_{1_{j_2}}, \ldots, \mu_{1_{j_k}}) \\ \Rightarrow \quad m = min\ \{x : Pr(f_j(N(x,\sigma_j^2), s(j_1), s(j_2)\ldots) \leq U_j) \geq Y_j\} \\ \Rightarrow \quad (\ \forall k : Pr(f_j(N(k,\sigma_j^2), s(j_1), s(j_2)\ldots) \leq U_j) \geq Y_j : m \leq k\ ) \\ \Rightarrow \quad m \leq n$$

This contradicts (7). $G$ is thus shown to be a monotonic and a convergent transformation, such that $G(M_1) \leq G(M_2)$ for $M_1 \leq M_2$. ■

Theorem 2 shows that $G$ is a monotonic transformation with respect to the partial order $\leq$ defined on the gate-size vectors. According to lattice theory [14], a partially ordered set forms a *complete lattice* if it has a least upper bound and a greatest lower bound on any subset of its elements. A lattice is constructed of all gate-size vectors that satisfy the size constraints. The bottom element of the lattice is a gate-size vector, comprising gate-sizes of which are equal to their individual lower bounds given by physical and timing constraints. The top element of the lattice is a virtual gate-size vector, having at least one upper gate-size bound violation. It is a virtual vector as it is a mapping of all gate-size vectors in the partially ordered set with at least one upper size-bound violation. This makes the family of gate-size vectors with the $\leq$ relation a complete lattice. The existence of a fixpoint in the lattice is guaranteed by Knaster and Tarski's theorem [14].

The iterative method (also called *successive approximation*) is often used to find a fixpoint. In this method, one

selects an initial solution $X_0$ and iteratively computes $X_1 = G(X_0), X_2 = G(X_1), \ldots$ in the hope of finding an $X_n$ such that $X_n = G(X_n)$. But the hope can not be fulfilled by starting from any initial point. Fortunately the bottom and the top elements are good candidates for that.

Following a tradition in lattice theory, $\perp$ and $\top$ are used to represent the bottom and top elements of the complete lattice respectively. $\perp = (l(i_1), l(i_2), \ldots, l(i_n))$, where $l(i)$ denotes the minimum gate-size for the driving gate of net $i$ as defined earlier. Since $\perp \leq G(\perp)$, based on the monotonic property of $G$, there is an ascending chain $\perp \leq G(\perp) \leq G^2(\perp) \leq \cdots$. If the chain has only finite elements, which is true on any finite solution space, the process eventually reaches a fixpoint. The only property that is used of $\perp$ is $\perp \leq G(\perp)$. Consequently, any solution $X_0$ such that $X_0 \leq G(X_0)$ can be used as an initial solution to reach a fixpoint. It is needed to find the least fixpoint, and can be done by starting with $\perp$ element. The solution obtained is the optimal one if the fixpoint reached is indeed a lower bound on all fixpoints of $G$.

*Theorem 3:* If $fix(G) = \{M_{f_1}, M_{f_2}, \ldots, M_{f_l}\}$ denotes the set of fixpoints of $G$, then there exists a lower bound fixpoint $M_{f_L} \in fix(G)$ called the least fixpoint, such that $(\forall j : 0 \leq j \leq l : M_{f_L} \leq M_{f_j})$.

*Proof:* The least fixpoint is defined as

$$M_{f_L} \stackrel{\triangle}{=} (i : 0 \leq i < n : \mu_{i_{f_L}})$$

where $\mu_{i_{f_L}} = min(\mu_{i_{f_1}}, \mu_{i_{f_2}}, \ldots \mu_{i_{f_l}})$. Gate-size vector $M_{f_L}$ is thus a lower bound on all the fixpoints, but it is necessary to show that $M_{f_L} \in fix(G)$ to prove the theorem. From (8), it is known that sizing down driving-gate sizes of nets coupled to a net $i$ does not decrease the probability of net $i$ satisfying its noise constraint. It is to be shown that the probability of a net $i$ satisfying its noise constraint is lower bounded by $Y_i$, when gate-sizes of the circuit are given by $M_{f_L}$ . From the definition of $M_{f_L}$, there must exist a fixpoint $M_{f_j}$ with the same driving-gate size for net $i$, such that $\mu_{i_{f_L}} = \mu_{i_{f_j}}$ and $(\forall k : 0 \leq k < n, k \neq i : \mu_{k_{f_j}} \geq \mu_{k_{f_L}})$. Since $M_{f_j}$ is a fixpoint, it satisfies the yield constraint. Given the monotonic properties of the noise function, $M_{f_L}$ must also satisfy the yield constraint. Additionally transformation $G$ on $M_{f_L}$ will yield $M_{f_L}$, since it is the lower bound on all fixpoints. It is thus a fixpoint of $G$, and is called the least fixpoint. ■

*Corollary 3.1:* The fixpoint reached starting from the $\perp$ element of the lattice is the least fixpoint and is the solution to the yield driven gate-sizing problem, provided the fixpoint $\neq \top$, which implies no solution.

The least fixpoint yields the minimal size of gates which achieve the local yield constraints and thus is the solution to the yield driven gate-sizing problem.

### B. Scheme of Chaotic Iterations

Before a good iterative order for updates is defined, it is important to establish its theoretical validity. The scheme of *chaotic iterations* [15] ensures that the process will always converge to the same fixpoint, irrespective of the order being used. Transformation $G$ is composed of a set of partial transformations $g_1, g_2, \ldots, g_n$. In each step, one or more partial transformations are applied to update the driving-gate sizes for some nets. Driving-gate sizes of all other nets are kept the same. $G_A$ is used to represent such a partial transformation done in one step, where $A$ represents the points where gate-sizes are updated.

*Lemma 1:* If $X \leq G(X)$, then $X \leq G_A(X) \leq G(X)$; if $X \geq G(X)$, then $X \geq G_A(X) \geq G(X)$.

The above lemma states that no matter what evaluation order is used, the generated sequence is monotonic in the same direction and it will not overshoot the fixpoint generated by $G$. This guarantees reaching the same fixpoint irrespective of the iteration scheme, starting with the same initial point in the lattice.

## IV. Iterative sizing algorithm

The following iterative algorithm is proposed. Layout extraction is performed on a given circuit and is used to construct the corresponding coupling-graph. Timing budgeting is performed on the circuit to further constrain the gate-size bounds which are initially given only by physical constraints. This incorporates the timing constraints of the circuit into the optimization process. The nominal driving-gate size of each net corresponding to a node in the coupling-graph is then initialized to its lower size-bound. Graph traversal is performed using a queue which is initially filled with nodes having $Pr(\eta(i) \leq U_i) < Y_i$. As a node $i$ is popped from the queue, its driver is sized up so that the yield constraint is met. All nodes having an edge from node $i$ are pushed in the queue, if they violate their yield constraints and are not already in the queue. Iteration stops either when the queue is empty, or when any nominal driver size exceeds the given constraint. In the latter case, no solution is concluded. Alternately, traversal may continue to try fixing other violations. In this way, updates are performed iteratively until the probability of no noise violations on each node is at least the local desired yield, or it is found that gate-sizing cannot achieve the local yield constraints.

The probability of a net satisfying a given noise constraint is evaluated from the distribution of coupling-noise induced on it. Analytical estimation of this distribution is not trivial. Given that the distributions are known, it is also needed to determine minimal nominal driving gate-sizes ($g_i$) of nets for noise-optimization under yield and size constraints. Both the analysis and optimization steps are difficult to solve analytically. Monte Carlo simulations are thus performed to estimate and determine noise distributions and optimal gate-sizes respectively. For the updates, the noise on a node $i$ is calculated based on the noise-model used. Nodes that have a direct edge to node $i$ induce coupling-noise on node $i$ and are used to determine the value of $\eta(i)$. If the $Pr(\eta(i) \leq U_i) < Y_i$, the driving-gate of $i$ is optimally sized to $g_i$ such that $Pr(\eta(i) \leq U_i) \geq Y_i$. The value of $g_i$ is evaluated using binary search and Monte Carlo simulations are used to determine if the current gate-size satisfies the noise constraints on all its driven nets. No

- Algorithm: Post-route yield driven gate-sizing for coupling-noise reduction
- **Input:** Layout extraction results
- **Output:** Optimal gate-sizes, if solution exists
- begin
  1) construct coupling-graph $G$ based on layout extraction
  2) perform timing budgeting on circuit to obtain size bounds
  3) initialize all nominal driver-sizes to their minimum ($\forall i : 0 \leq i < n : \mu_i = l(i)$)
  4) while ( Pr(Noise constraint met for node $i$) $< Y_i$) for any node $\wedge$ each nominal gate-size $\leq$ its upper bound ($\forall i : \mu_i \leq u(i)$)
  5) for each node $i$ violating the yield constraint ($Pr(\eta(i) \leq U_i) < Y_i$)
  6) use Monte Carlo simulations to determine $\mu_i = g_i(\mu_{i_1}, \ldots, \mu_{i_k})$
- end

Fig. 1. Post-route yield driven driver-sizing algorithm for Coupling-Noise reduction

update is performed if the calculated probability is already more than $Y_i$. If the sizing up violates size constraints, no solution to achieving the desired yield is declared. Optionally, iterations may be further done to achieve the desired yield in other nets. The order of the iterations may only alter the rate of convergence, but the algorithm is guaranteed to reach the solution in any case, provided it exists. The pseudo-code of the proposed algorithm is shown in Figure 1.

## V. Results

Experimental results of the proposed algorithm are presented for the ISCAS'85 benchmarks [11] and three larger circuits. Parameters for the circuits are randomly generated with realistic values in a $0.18\mu m$ technology (The driver resistance $R_d$ is from 20 to 2000$\Omega$, loading capacitance $C_l$ is from 4 to 50fF, and the slew is from 10 to 300ps). The $2\pi$ model [16] is used for noise modeling. Gate-sizes are bounded in each direction by a factor of at most 2 for physical constraints and their effective driver resistances are considered as Gaussian random variables. Circuits are simulated for two variance values $\sigma_1^2$ and $\sigma_2^2$, with $3\sigma$ values set to $10\%$ and $15\%$ of the nominal respectively. Monte Carlo simulations are performed with 1000 and 10000 samples. The error between the results for the two samples is found to be less than $2\%$. The maximum tolerable noise ($U_i$) for a net is set to $0.2V_{dd}$.

Obtained results are compared with those obtained by using the optimal gate-sizing algorithm [8]. Additionally, results are presented for a modified optimal gate-sizing algorithm where gates are sized more than their optimal values to account for uncertainty. This method employs guard-bands (GB) to size up the driving-gate of a net $i$ for noise bound lower than its actual noise bound $U(i)$. Since the optimization is conservative, it is expected that the circuit will have a high probability of satisfying the noise constraints on its nets under uncertainty. Results are presented for GB values of $2\%$ and $3\%$ safety respectively. The algorithms which do not consider process variations directly are denoted as *WoPV* algorithms with a given GB value. The proposed yield driven gate-sizing algorithm is denoted as *WPV*.

Table I shows the the number of nets, the number of edges in the coupling-graph formed, the total number of initial noise violations, and run times for the *WoPV* and *WPV* algorithms (with 1000 Monte Carlo samples). The number of initial violations denote the number of coupling-noise violations in the given circuit before the gates are sized down. Run times for the three *WoPV* algorithms are almost identical. The *WoPV* algorithm without any guard band [8] successfully removes noise violations for the circuits.

Tables II and III present global yield values obtained by the algorithms for variances of $\sigma_1^2$ and $\sigma_2^2$ respectively. Global yield in circuits where optimal gate-sizing cannot remove all noise violations would be $0\%$ since even a single violation fails the circuit. The algorithms are thus tested on circuits whose noise violations can be removed by gate-sizing. All algorithms can however optimize circuits partially when the yield constraint cannot be globally met.

It is observed that the gate-size vector given by the optimal gate-sizing algorithm is very sensitive to variations. The *WoPV* algorithms with GB perform better but produce lower yields when variations are increased. Larger GB values seem helpful, but do not necessarily produce a solution. This is observed in $CKT\_3$ where the *WoPV* algorithm fails to produce a solution for a $3\%$ value of GB. Higher values of GB also translate to larger gate-sizes which is attained to minimize. The

TABLE I
Benchmarks with Initial Violation figures and Run Times

| Circuit | # of Nets | # of C Edges | # of Initial Violations | Run Times(s) | |
|---|---|---|---|---|---|
| | | | | WoPV | WPV |
| C17 | 12 | 22 | 1 | 0.01 | 0.41 |
| C432 | 336 | 566 | 3 | 0.01 | 2.55 |
| C499 | 408 | 653 | 3 | 0.01 | 3.23 |
| C880 | 729 | 1253 | 5 | 0.01 | 5.49 |
| C1355 | 1064 | 1669 | 6 | 0.01 | 6.27 |
| C1908 | 1498 | 2677 | 9 | 0.01 | 9.48 |
| C2670 | 2076 | 3854 | 12 | 0.01 | 14.3 |
| C3540 | 2939 | 5042 | 11 | 0.01 | 18.78 |
| C5315 | 4386 | 7059 | 8 | 0.02 | 23.11 |
| C6288 | 4800 | 7213 | 13 | 0.01 | 23.40 |
| C7552 | 6144 | 10965 | 16 | 0.02 | 35.80 |
| CKT_1 | 20K | 39155 | 42 | 0.09 | 133.81 |
| CKT_2 | 32K | 62768 | 61 | 0.16 | 185.12 |
| CKT_3 | 40K | 63222 | 44 | 0.17 | 255.94 |

TABLE II

GLOBAL YIELD VALUES OBTAINED WITH VARIANCE $\sigma_1^2$ BY THE ALGORITHMS FOR ALL BENCHMARKS

| Circuit | % Global Yield | | | |
|---|---|---|---|---|
| | WoPV | | | WPV |
| | 0% GB | 2% GB | 3% GB | $Y_i$ = 0.98 |
| C17 | 51 | 95 | 97 | 100 |
| C432 | 2 | 89 | 98 | 100 |
| C499 | 2 | 84 | 93 | 99 |
| C880 | 0 | 82 | 96 | 99 |
| C1355 | 0 | 95 | 100 | 100 |
| C1908 | 0 | 75 | 97 | 100 |
| C2670 | 0 | 83 | 97 | 100 |
| C3540 | 0 | 64 | 94 | 97 |
| C5315 | 0 | 91 | 99 | 99 |
| C6288 | 0 | 84 | 100 | 100 |
| C7552 | 0 | 73 | 97 | 99 |
| CKT_1 | 0 | 41 | 91 | 100 |
| CKT_2 | 0 | 47 | 93 | 96 |
| CKT_3 | 0 | 62 | 0 | 94 |

TABLE III

GLOBAL YIELD VALUES OBTAINED WITH VARIANCE $\sigma_2^2$ BY THE ALGORITHMS FOR ALL BENCHMARKS

| Circuit | % Global Yield | | | |
|---|---|---|---|---|
| | WoPV | | | WPV |
| | 0% GB | 2% GB | 3% GB | $Y_i$ = 0.98 |
| C17 | 50 | 89 | 92 | 100 |
| C432 | 2 | 67 | 95 | 95 |
| C499 | 0 | 51 | 86 | 94 |
| C880 | 0 | 52 | 85 | 88 |
| C1355 | 0 | 75 | 97 | 94 |
| C1908 | 0 | 46 | 75 | 92 |
| C2670 | 0 | 40 | 81 | 82 |
| C3540 | 0 | 25 | 70 | 84 |
| C5315 | 0 | 55 | 93 | 92 |
| C6288 | 0 | 62 | 92 | 92 |
| C7552 | 0 | 43 | 78 | 86 |
| CKT_1 | 0 | 2 | 59 | 82 |
| CKT_2 | 0 | 2 | 65 | 83 |
| CKT_3 | 0 | 9 | 0 | 78 |

results demonstrate that the *WPV* algorithm produces higher yields and very minimal area overhead. The *WPV* algorithm is also more efficient in terms of area overhead as compared to *WoPV* with $3\%$ GB. Since the optimization is performed only once at the post-route stage, the runtime increase of the *WPV* algorithm over the others is acceptable. The results validate the effectiveness of the yield driven gate-sizing algorithm. Results reported are for simulations run on a P-IV $1.6GHz$ Dell Latitude laptop, with Debian Linux 3.0 and 128Mb RAM.

## VI. CONCLUSIONS AND FUTURE WORK

The paper presents a post-route gate-sizing algorithm for coupling-noise reduction which constrains the local yield loss under process variations. Experimental results on the ISCAS and larger benchmarks validate the claim by comparisons to traditional approaches. The proposed algorithm can be used consistently for continuous or discrete gate-sizing. Statistical methods for determining the distribution of noise functions under uncertainty would be considered in the future. It shall eliminate the use of Monte Carlo simulations in the inner loop of the algorithm.

TABLE IV

NORMALIZED SUM OF GATE SIZES USED AS AN AREA METRIC OBTAINED BY THE ALGORITHMS FOR ALL BENCHMARKS

| Circuit | Area (Normalized) | | | |
|---|---|---|---|---|
| | WoPV | | | WPV |
| | 0% GB | 2% GB | 3% GB | $Y_i$ = 0.98 |
| C17 | 100000 | 100438 | 100634 | 101184 |
| C432 | 100000 | 100042 | 100068 | 100082 |
| C499 | 100000 | 100048 | 100074 | 100090 |
| C880 | 100000 | 100052 | 100079 | 100080 |
| C1355 | 100000 | 100036 | 100058 | 100046 |
| C1908 | 100000 | 100022 | 100037 | 100037 |
| C2670 | 100000 | 100031 | 100049 | 100043 |
| C3540 | 100000 | 100000 | 100044 | 100041 |
| C5315 | 100000 | 100028 | 100017 | 100014 |
| C6288 | 100000 | 100011 | 100016 | 100013 |
| C7552 | 100000 | 100010 | 100024 | 100020 |
| CKT_1 | 100000 | 100015 | 100021 | 100019 |
| CKT_2 | 100000 | 100013 | 100013 | 100011 |
| CKT_3 | 100000 | 100005 | 0 | 100008 |

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