Impact of Modern Process Technologies on the Electrical Parameters of Interconnects

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***Abstract*— This paper presents the results obtained from an experimental study of the impact of modern process technologies on the electrical parameters of interconnects. Variations in parasitic capacitances and resistances due to dummy metal fills, chemical mechanical polishing, multiple thin inter-layer dielectrics and trapezoidal conductor cross-sections are presented. Accurate variations in the parasitics are reported for a set of timing critical nets using 3d field solvers for extraction. Results obtained on a set of industrial designs show that the impact of dummy fills and trapezoidal conductor cross-sections are significant.**

I. Introduction

With CMOS feature sizes scaling down to the deep sub-micron regime, there has been a tremendous growth in the number of transistors and the complexity of modern ICs. The integration of numerous active elements within an IC necessitates that it features nine or more layers of high density metal interconnect. The electrical parameters of these interconnects (primarily the resistance and capacitance) critically determine the timing characteristics of the circuit. Modern processing techniques are employed at Back-End Of Line (BEOL) manufacturing process to improve manufacturability of interconnects.

Starting from the 180nm generation, the semiconductor industry has transitioned from using aluminum interconnect metal to copper interconnect metal. This has been motivated by the lower resistivity and higher reliability of copper in comparison to aluminum. In contrast to an aluminum interconnect metal process, the oxide between the metal layers is patterned instead of the metal for a copper interconnect process, as copper is more difficult to etch than aluminum.

Chemical-mechanical polishing or planarization (CMP) is performed to achieve uniformity of conductor and dielectric thickness in the manufacturing process. For copper interconnect, the underlying metal is polished during CMP. This is also known as the *damascene CMP* process. Although CMP provides good local planarization, it is unable to guarantee global uniformity due to multiple factors including planarization length, underlying non uniform pattern density and feature perimeter sum [1] [2]. A density range design rule is therefore employed to equilibrate density and limit metal thickness variability due to CMP. This is achieved by insertion of *dummy fill* metal structures in the empty regions of each metal layer [3]. Although dummy fill insertion improves the uniformity of metal feature density and enhances the planarization that can be obtained by CMP, it contributes to increased coupling capacitances, and thereby increased total capacitances of the interconnects.

Modern BEOL manufacturing processes additionally employ multiple layers of low-k dielectrics between metal layers, instead of the traditional uniform Silicon-Dioxide dielectric. Most low-k porous dielectrics are hydrophobic and fragile in character, and it is critical that the surface hard mask, located on the top of the Inter Level Dielectric (ILD) stack, shield them during CMP. These multiple, thin dielectrics affect the parasitic capacitances between the metal lines. Furthermore, due to the presence of these thin surface hard masks of different dielectric permittivity, the overall dielectric stack has more ILDs, thereby stressing capacitance extractors.

The etching process during manufacturing can also cause significant variations in interconnect patterns, not only along the x-y plane but also on the side-walls. Thereby, the interconnect cross-sections are increasingly trapezoidal in nature [4]. With the reduction in spacing between interconnects and the interconnects themselves becoming narrower and longer, the effects of etching and trapezoidal shapes on the electrical parameters can no longer be neglected.

With an increasing significance of variability-driven considerations in the design of interconnects for modern circuits, it is important to determine the effect of the above factors on the electrical parameters of interconnects [5]. In this paper, we employ accurate industrial parasitic extractors and simulators to quantify variations on the interconnect resistance and capacitance in a set of industrial benchmarks. Technology and process parameters are obtained from two foundries. Experimental results are obtained for a set of industrial designs.

The rest of this paper is organized as follows. Section II presents a brief description of multiple modern process technologies on interconnects. We present the impact of each of these technologies and factors using experimental results in Section III. Conclusions are discussed in Section IV.

II. Modern process technologies

A. Dummy fill insertion

Dummy fills are floating (or grounded) metal objects inserted in each metal layer of the design to satisfy given design density rules for

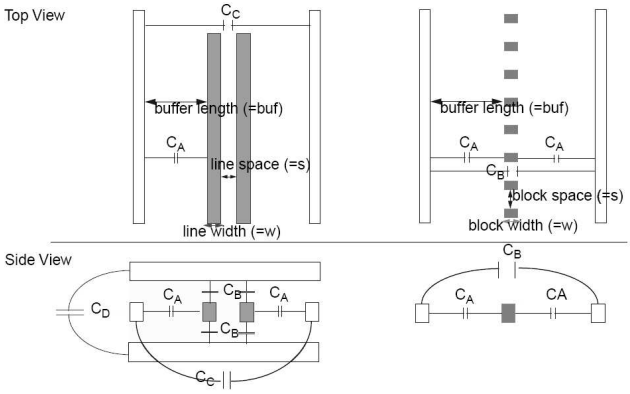

Fig. 1. Increased interconnect capacitances due to fills

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the BEOL manufacturing process and to enhance the planarization obtained by CMP [6]. However, they cause additional coupling capacitances as shown in Figure 1. In this figure, the interconnects are shown as white rectilinear boxes, while the shaded objects represent the fills. These additional capacitances depend on factors like fill patterns, minimum inter-fill spacing and minimum conductor-to-fill spacing values.

B. Chemical mechanical polishing

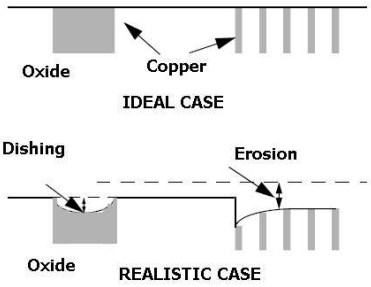

Fig. 2. Dishing and erosion caused by CMP

Systematic variations in the metal thickness following a damascene CMP process due to factors like planarization length, layout density and perimeter sum cause *dishing* and *erosion* of interconnects (Figure 2). There is a high amount of dishing for wide lines, and erosion increases with increasing metal pattern density. Erosion generally dominates dishing for fine pitched lines, specially at high density [7]. Dishing and erosion may cause defocus issue in the lithography process following CMP and therefore is a concern from manufacturability perspective. They can also cause interconnect resistance and capacitance variations due to changes in interconnect cross-section.

C. Multiple thin dielectrics

Modern manufacturing process employ multiple ILDs between vertically adjacent metal layers. The use of low-k dielectrics help in reducing the parasitic capacitances for the interconnects. However, these soft dielectrics are shielded using surface hard masks (typically large-k dielectrics) to aid planarization obtained by CMP.

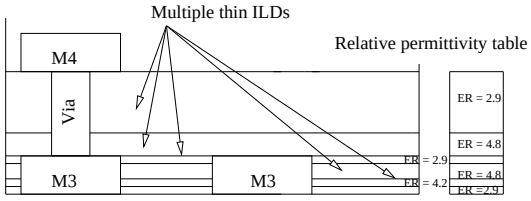

Fig. 3. Vertical profile for a given process

For example, Figure 3 shows a vertical profile between two metal layers featuring six ILDs. Parasitic extractors often assume a single homogeneous ILD since extraction with multiple ILDs is time consuming. However, this introduces inaccuracies in the extracted interconnect capacitances. In our experiments, we replace the dielectric stack between every two adjacent metal regions, as shown in Figure 3, with a corresponding homogeneous dielectric with permittivity equal to the weighted average of permittivities of individual ILD layers between the metal regions. The weighting factor is taken as the thickness of the ILD layer. In other words, if $\epsilon_1, \epsilon_2, \ldots, \epsilon_k$ are the permittivities of ILDs with $d_1, d_2, \ldots, d_k$ being their thickness, the permittivity of homogeneous dielectric is taken as $\epsilon = \frac{\sum_{i=1}^{k} \epsilon_i . d_i}{\sum_{i=1}^{k} d_i}$.

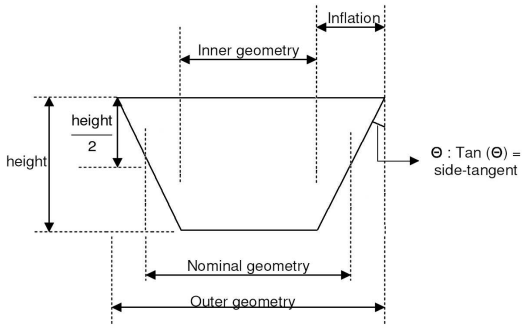

Fig. 4. Trapezoidal interconnect cross-section specification

D. Trapezoidal conductor cross-sections

Interconnect cross-sections for modern day ICs are better approximated as trapezoids than rectilinear geometries. Such variations in the interconnect cross-section directly impacts its parasitic capacitance and the resistance. However, capacitance extraction tools use rectilinear geometries for efficiency purposes. To retain the efficiencies, trapezoidal conductors are often specified by their *nominal geometry*, which is rectilinear, and a *side-tangent*, which captures the slope. Figure 4 shows the specification for a trapezoidal conductor cross-section. Often trapezoidal conductor cross-sections are approximated to a staircase of rectilinear geometries, but at the expense of increased memory usage and run-times.

III. Impact of modern process technologies

In this section, we present our experimental flow and the impact of each of the mentioned process technologies on a set of designs implemented in 90nm technology. Some of the designs are testcases obtained from Opencores [8]. In addition, we use a few real industrial testcases ($cust1$, $cust2$) in our flow.

We use a commercial, fast extraction tool to extract parasitics from connected databases that represent integrated circuit layout designs. For each design, the extracted parasitics, the synthesized library information and the design gate-level netlist is submitted to a commercial timing analysis tool. Timing analysis of the design with given timing constraints produces a set of (*50* for our experiments) most critical paths. We denote the nets lying on these critical paths as the critical nets for that design. Extremely accurate parasitic extractors using field solvers are employed to extract the electrical parameters for these critical nets, since these tools are relatively slow and it is impractical to employ them for parasitic extraction for the entire design.

For each design, we run the above flow for a base case, which does not contain dummy fills and considers process specified nominal metal and ILD thickness. The nominal thickness for the metal layers do not represent the pre-CMP thickness, but a mean value assuming CMP achieves uniform global planarization. The true thickness for a layer at any point could therefore be either more or less than the nominal value. Vertically adjacent metal layers are assumed to be separated with a single ILD, with a uniform dielectric constant. Finally, the base case considers rectilinear conductors (nominal geometries in Figure 4). For each design, we denote the timing critical nets obtained from its base case as the critical nets for that design. Table I presents the set of designs used in our experiments. For each design, we report the total number of nets, number of critical nets and its size.

TABLE I
DESIGN CHARACTERISTICS

Design	# total nets	# critical nets	Area ($\mu m \times \mu m$)
add16	63	19	22 × 22
risc16	1226	61	135 × 135
cordic	2526	121	199 × 199
usb	8082	101	248 × 248
fpu	9163	1034	260 × 260
cust1	28332	177	504 × 504
des	48737	161	734 × 734
cust2	35382	349	743 × 750

TABLE II
IMPACT OF DENSE FILLS (ALL NETS)

Design	Total cap variation (%)			
	μ	σ	max	min
add16	48.1	18.9	110.4	15.4
risc16	45.2	30.0	232.4	-7.3
cordic	54.9	32.8	222.7	-4.8
usb	32.7	23.6	182.0	-19.7
fpu	32.2	25.6	266.8	-21.9
cust1	31.1	22.5	191.8	-23.0
des	42.0	30.1	266.8	-21.5
cust2	15.0	12.4	144.0	-24.0

TABLE III
IMPACT OF SPARSE FILLS (ALL NETS)

Design	Total cap variation (%)			
	μ	σ	max	min
add16	21.4	9.6	48.5	4.0
risc16	14.4	14.0	136.6	-12.0
cordic	18.9	17.0	117.2	-12.1
usb	7.8	9.7	109.4	-20.5
fpu	9.1	12.3	111.4	-29.1
cust1	5.6	7.1	75.9	-22.9
des	12.3	13.2	122.9	-32.5
cust2	3.6	5.2	72.3	-25.3

A. Impact of fills

We present the impact of dummy fill insertion on parasitic capacitances in this section. For each design, we generate dummy fills using a commercial Placement and Routing tool and set the minimal fill-to-metal spacing for a given metal layer to the same as the inter metal spacing for that layer. We denote this design with fills as the design with *dense* fills. In addition, we generate dummy fills in the base design with minimal fill-to-metal spacing for a given metal layer as twice the minimal inter metal spacing for that layer and term this design as the design with *sparse* fills. The experimental flow is run for the designs with *dense* and *sparse* fills respectively. Since fill insertion does not directly impact the parasitic resistance of an interconnect, we present results obtained for resistance variations due to CMP based on underlying fill patters in the next section.

The extracted lumped capacitance of a net is termed as its *Wire cap* and includes its self and coupling capacitances. The sum of all capacitances on each of the pin the net connects to (that is, the driver and loading gate capacitances) is termed as the net's *Pin cap*. The sum of the net's *Wire cap* and *Pin cap* is termed as the *Total cap* of that net.

Mathematically, the wire and total capacitance variation due to dummy fills is computed as the following.

$$\%C\_var_{fills}^{Wire} \triangleq \frac{C_{fills}^{Wire} - C_{base}^{Wire}}{C_{base}^{Wire}} \times 100.0 \quad (1)$$

$$\%C\_var_{fills}^{Total} \triangleq \frac{C_{fills}^{Total} - C_{base}^{Total}}{C_{base}^{Total}} \times 100.0 \quad (2)$$

Note that process technologies do not affect interconnect *Pin caps*.

Tables II and III present the *Total cap* variations for all nets due to *dense* and *sparse* fills respectively obtained using the fast parasitic extractor. For each design, we present the mean variation (μ), the standard deviation of the variation (σ) and the *max* and *min* variation respectively. From these tables, we infer that *dense* and *sparse* fills cause an increase in the total capacitance of an interconnect by 37% and 11% respectively, on the average over all designs. We also observe that fills can cause as high as a 2.6X increase on the total capacitance of an interconnect (design *des* due to *dense fills*).

TABLE IV
IMPACT OF DENSE FILLS (CRITICAL NETS)

Design	Wire cap variation (%)				Total cap variation (%)			
	μ	σ	max	min	μ	σ	max	min
add16	104.0	35.8	195.0	39.3	49.9	24.7	114.6	11.3
risc16	80.5	28.1	160.0	5.1	52.6	29.0	133.4	0.1
cordic	84.9	31.7	208.7	9.2	48.3	28.0	142.6	0.8
usb	46.1	19.9	108.4	9.1	34.9	20.7	102.0	1.5
fpu	72.0	29.9	217.8	2.2	32.2	18.1	141.8	0.3
cust1	50.8	29.5	219.4	-1.3	31.3	26.5	146.5	-0.3
des	76.2	31.3	154.5	5.1	53.1	32.3	126.9	1.0
cust2	33.1	15.2	97.4	2.1	15.4	13.6	67.5	0.0

TABLE V
IMPACT OF SPARSE FILLS (CRITICAL NETS)

Design	Wire cap variation (%)				Total cap variation (%)			
	μ	σ	max	min	μ	σ	max	min
add16	31.0	11.5	52.9	8.6	14.9	7.9	36.0	2.4
risc16	20.4	9.7	48.0	3.4	13.3	8.7	44.2	0.1
cordic	21.6	13.0	77.0	2.1	12.3	9.5	51.0	0.0
usb	7.7	5.8	25.4	0.3	5.9	4.8	19.6	0.1
fpu	16.0	10.0	88.0	-2.1	7.1	5.6	62.3	-0.7
cust1	7.7	8.0	65.4	-3.0	4.7	5.8	43.7	-0.7
des	18.6	11.2	58.4	-3.0	12.8	9.3	45.0	-0.9
cust2	7.5	6.0	35.5	-5.7	3.6	4.2	27.7	-0.8

Tables IV and V present accurate *Wire cap* and *Total cap* variations obtained from the field solver for the timing critical nets of each design. Results from accurate capacitance extraction show that although maximal wire capacitance variations can exceed 200%, the total capacitance variation is constrained because of the unaffected pin capacitances to less than 150%. We evaluate from these tables that on the average, the mean *Wire cap* and the *Total cap* variations for the designs with *dense* fills are 68% and 40% respectively. These numbers for the design with *sparse* fills are evaluated to be 16% and 9% respectively.

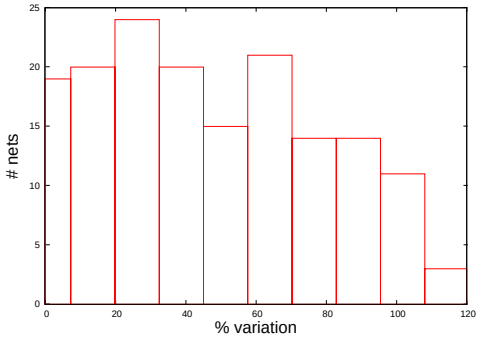

Fig. 5. Accurate impact of dense fi lls on total cap for timing critical nets (design *des*)

Figure 5 shows the distribution of the $\%$ *Total cap* variation for the timing critical nets of the design *des* due to *dense fills*. The X-axis shows eleven uniformly spaced $\%$ *Total cap* variation buckets over

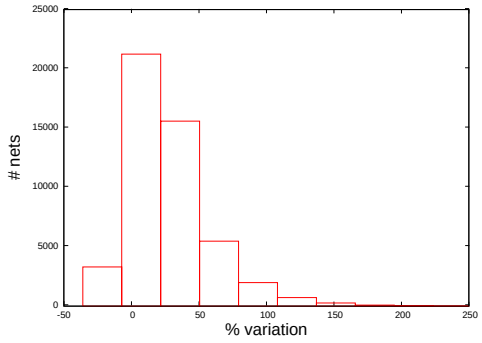

Fig. 6. Impact of dense fills on total cap for all nets (design *des*)

the entire range of variation for the design. We plot the number of nets lying in a particular bucket (range of % *Total cap* variation) in the Y axis. We observe that the distribution is positively skewed with a mean variation of 31%. Similar plots showing the distribution of the % *Total cap* variation for all nets in the design *des* due to *dense fills* is presented in Figure 6.

B. Impact of CMP

We use a prototype industrial CMP simulator to obtain metal thickness variations for all layers in a design having dummy fills. The topographies obtained from the CMP simulator are fed to the field solver to obtain the impact of CMP on the resistance and capacitance of the timing critical nets. In the CMP simulation, we do not consider the effects of multi-layer accumulative topography variation on the metal thickness variations. The variations of dielectric thickness and relative height of metal lines due to the multi-layer accumulative topography variations are not considered either. Note that the base case here has dummy fills and assumes uniform metal thickness. We use this base case for comparison to a design having the same fill pattern but considering thickness variations due to CMP.

TABLE VI
IMPACT OF CMP WITH DENSE FILLS (CRITICAL NETS)

Design	Wire cap variation (%)				Total cap variation (%)			
	μ	σ	max	min	μ	σ	max	min
add16	0.2	0.9	2.0	-1.3	0.1	0.6	1.4	-0.8
risc16	0.1	0.8	2.4	-1.7	0.0	0.5	1.2	-1.6
cordic	-0.1	1.4	3.3	-3.5	-0.1	0.9	1.8	-2.4
usb	0.3	1.0	4.6	-2.5	0.2	0.6	2.2	-1.2
fpu	0.0	1.4	5.7	-4.3	0.0	0.8	2.9	-2.7
cust1	0.1	1.2	5.5	-3.2	0.1	0.6	1.9	-3.2
des	0.1	1.2	4.1	-5.4	0.1	0.7	2.2	-2.2
cust2	0.0	1.2	3.9	-5.9	0.0	0.5	1.3	-4.5

TABLE VII
IMPACT OF CMP WITH SPARSE FILLS (CRITICAL NETS)

Design	Wire cap variation (%)				Total cap variation (%)			
	μ	σ	max	min	μ	σ	max	min
add16	0.4	1.3	2.8	-1.8	0.1	0.9	1.7	-1.8
risc16	0.1	1.2	3.5	-2.9	0.1	0.8	3.5	-1.5
cordic	-0.1	1.5	3.1	-4.7	0.0	0.9	2.3	-2.8
usb	0.0	1.0	2.8	-4.9	-0.1	0.7	1.5	-2.7
fpu	0.0	1.7	6.1	-6.0	0.0	0.8	3.0	-4.0
cust1	0.0	1.4	4.5	-5.9	0.0	0.6	1.7	-1.7
des	0.2	1.3	4.5	-4.2	0.2	0.9	3.5	-2.6
cust2	0.0	1.2	3.7	-4.5	0.0	0.5	2.1	-3.0

Tables VI and VII present the *Wire cap* and *Total cap* variations due to CMP for designs having *dense* and *sparse* fills respectively. We observe that the variations in the wire and total capacitances due to CMP are negligible on the average, having a standard deviation of about 0.7%. We observe that the thickness variations caused due to CMP are small (5% – 10%). Similar thickness variations found for all metal layers explain the negligible impact of CMP observed. We present the distribution of the % *Total cap* variation on the critical nets with underlying *dense* fills for the design *des* in Figures 7 and 8.

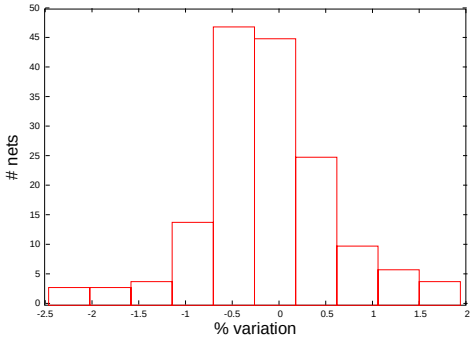

Fig. 7. Accurate impact of CMP (dense fills) on total cap for timing critical nets (design *des*)

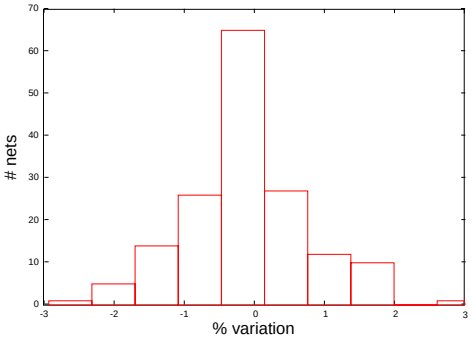

Fig. 8. Accurate impact of CMP (sparse fills) on total cap for timing critical nets (design *des*)

It is seen that the distributions are approximately symmetric around a 0% mean. The absolute maximal *Total cap* variation is found to be 4.5% (design *cust2*). However, note that the effects of dielectric thickness variations and relative height variations of metal lines on capacitance are not considered in our study.

The resistance between two given pins of a net is termed as its *Port* resistance. The resistance of the gate timing-arc that drives a given net is termed as the *Drive* resistance. The sum of the port and drive resistance is termed as the net's *Total* resistance. Tables VIII and IX present the variation in the port and total resistance for the critical nets in each design due to CMP with underlying *dense* and *sparse* fills respectively.

We observe that the total resistance variations due to CMP are not significant on the average. This is because the drive resistance is usually much larger than the port resistance. However, the absolute maximal variations observed in the total resistance are large (2.5% – 19.1%) for several designs (designs *add16*, *cust1* and *usb*). The variation in total resistances for the design *usb* is presented in Figures 9 and 10.

A detailed study of these designs shows that the drive resistance is in the same order as the port resistance on the net with the maximal total resistance variation. This variation may be large enough to cause a re-ordering of critical paths.

C. Impact of multiple thin dielectrics

We next consider variations in interconnect capacitances for a design having multiple ILDs (specifications obtained from the respective foundries) with respect to a base case which considers

TABLE VIII

IMPACT OF CMP WITH DENSE FILLS (CRITICAL NETS)

Design	Wire res variation (%)				Total res variation (%)			
	μ	σ	max	min	μ	σ	max	min
add16	9.1	3.0	12.4	-0.6	1.0	3.0	10.7	-0.6
risc16	8.4	0.9	10.8	5.3	0.0	0.0	0.1	0.0
cordic	6.3	1.0	8.7	4.4	0.0	0.0	0.1	0.0
usb	4.5	0.9	5.9	0.9	0.5	1.4	5.9	0.0
fpu	3.6	0.7	10.2	0.3	0.0	0.0	0.1	0.0
cust1	2.7	0.9	7.4	0.2	0.2	0.5	4.3	0.0
des	2.2	0.8	3.7	0.1	0.1	0.2	2.1	0.0
cust2	3.2	3.0	14.7	0.4	0.1	0.2	0.6	0.0

TABLE IX

IMPACT OF CMP WITH SPARSE FILLS (CRITICAL NETS)

Design	Wire res variation (%)				Total res variation (%)			
	μ	σ	max	min	μ	σ	max	min
add16	17.1	5.0	23.8	3.9	1.9	5.0	19.1	0.0
risc16	4.1	1.0	7.3	2.2	0.0	0.0	0.0	0.0
cordic	2.1	1.5	6.4	0.2	0.0	0.0	0.0	0.0
usb	-0.7	0.7	1.3	-2.2	0.0	0.2	1.3	-0.3
fpu	-0.2	0.7	9.5	-1.8	0.0	0.0	0.0	0.0
cust1	-1.6	1.0	7.1	-2.8	0.0	0.3	3.0	-2.5
des	-1.4	0.7	0.9	-2.7	0.0	0.1	0.0	-0.8
cust2	0.1	4.8	38.3	-7.2	0.0	0.1	0.1	-0.6

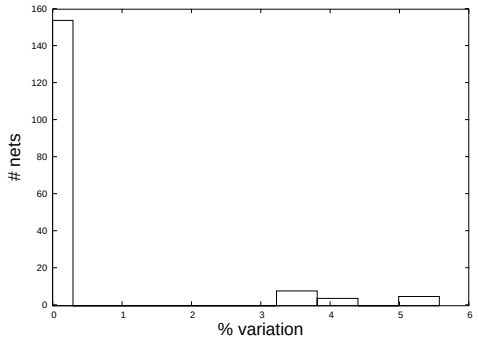

Fig. 9. Accurate impact of CMP (dense fills) on total res for timing critical nets (design *usb*)

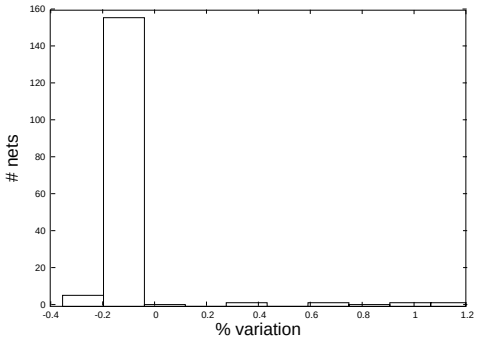

Fig. 10. Accurate impact of CMP (space fills) on total res for timing critical nets (design *usb*)

TABLE X

IMPACT OF MULTIPLE THIN DIELECTRICS (ALL NETS)

Design	Total cap variation (%)			
	μ	σ	max	min
add16	0.0	0.9	1.6	-2.4
risc16	0.6	0.7	7.5	-3.5
cordic	0.6	0.9	7.4	-6.9
usb	0.4	0.7	6.1	-6.1
fpu	0.4	0.6	10.8	-4.2
cust1	0.4	0.7	4.8	-11.7
des	0.4	0.6	8.6	-6.4
cust2	0.0	0.9	7.5	-11.2

TABLE XI

IMPACT OF MULTIPLE THIN DIELECTRICS (CRITICAL NETS)

Design	Wire cap variation (%)				Total cap variation (%)			
	μ	σ	max	min	μ	σ	max	min
add16	-1.8	1.3	1.2	-4.2	-0.7	0.6	0.6	-1.7
risc16	-2.3	1.2	1.8	-4.8	-1.4	0.9	0.5	-3.2
cordic	-2.6	1.8	5.4	-8.0	-1.3	1.2	2.7	-6.8
usb	-2.8	1.6	0.2	-10.1	-2.0	1.3	0.2	-5.8
fpu	-2.0	1.1	2.0	-6.6	-0.8	0.6	0.5	-5.5
cust1	-2.6	1.3	0.6	-7.0	-1.4	1.1	0.5	-6.0
des	-2.2	1.9	5.7	-9.2	-1.5	1.5	1.5	-8.6
cust2	-1.8	2.2	5.8	-8.5	-0.9	1.3	3.9	-8.2

average single ILDs. The dielectric constant of the single ILD in a region is determined by a thickness weighted average of the dielectric constants of the specified multiple ILDs in that region. Single ILDs are computed for each region comprising of a routing layer (metal/poly) and the via layer above it using the approximation described in Section II-C. For example, a single ILD would be computed for the region starting from the bottom level of metal layer 'M3' to the bottom level of the metal layer 'M4' in Figure 3.

We observe negligible impact of the assumption of a single ILD for faster extraction over all nets in Table X (obtained from the fast parasitic extractor) on the average. Table XI presents very accurate wire and total capacitance variations on the critical nets of each design (obtained from the field solver). From Table XI, we infer that the assumption of averaged ILDs between metal layers overestimates the total net capacitances by 1.4% on the average.

Figures 11 and 12 present the distribution of the *Total cap* variations on all nets and critical nets respectively for design *des*. The distributions are found to be negatively skewed.

D. Impact of etching and trapezoidal conductor cross-sections

We consider the impact of trapezoidal cross-sections and etching of conductors on interconnect parasitics in this section. We extract parasitics of a design considering the specifications for the outer and nominal geometries and the side tangent (Figure 4) obtained as functions of metal thickness and density from respective foundries. The extracted parasitics are compared to those of a base case that considers only nominal geometries and does not consider effects caused due to etching and trapezoidal conductor cross-sections.

We present the total capacitance variation observed for all nets in Table XII (obtained from the fast parasitic extractor). Table XIII presents very accurate wire and total capacitance variations on the critical nets of each design (obtained from the field solver). The library used by design *cust2* does not have any trapezoidal cross-

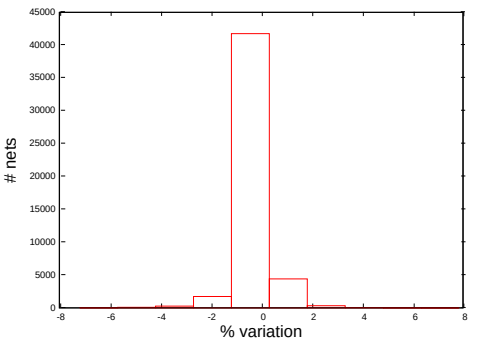

Fig. 11. Impact of thin dielectrics on total cap for all nets (design *des*)

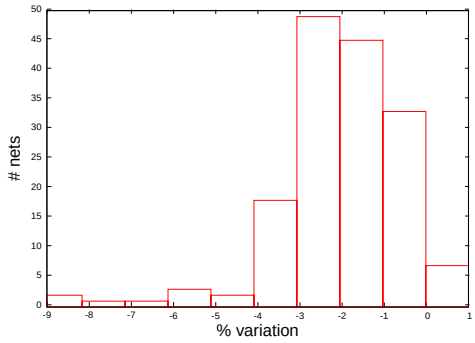

Fig. 12. Accurate impact of thin dielectrics on total cap for timing critical nets (design *des*)

TABLE XII
IMPACT OF ETCH AND TRAPEZOIDAL CROSS-SECTIONS (ALL NETS)

Design	Total cap variation (%)			
	μ	σ	max	min
add16	2.3	1.9	6.8	-1.6
risc16	5.9	3.0	16.6	-5.3
cordic	4.7	3.0	19.2	-4.7
usb	7.1	3.8	21.6	-6.2
fpu	5.3	3.2	19.1	-6.2
cust1	7.1	4.1	23.8	-3.0
des	6.2	3.2	22.0	-5.4
cust2	2.5	2.5	18.4	-5.6

TABLE XIII
IMPACT OF ETCH AND TRAPEZOIDAL CROSS-SECTIONS (CRITICAL NETS)

Design	Wire cap variation (%)				Total cap variation (%)			
	μ	σ	max	min	μ	σ	max	min
add16	16.1	3.9	23.6	9.6	7.4	4.1	20.2	2.2
risc16	18.6	3.6	30.9	10.1	11.1	5.4	20.8	0.6
cordic	18.1	4.2	31.4	9.1	9.8	5.1	26.2	0.3
usb	22.6	4.2	33.2	9.6	16.3	7.4	29.8	0.9
fpu	18.9	3.8	34.6	6.5	7.6	3.0	23.9	0.2
cust1	21.4	4.1	31.7	11.2	11.2	6.7	26.6	0.7
des	18.3	4.1	29.9	6.5	11.8	5.8	28.0	0.3
cust2	17.9	3.4	26.6	6.8	7.6	5.7	25.4	0.1

sections.

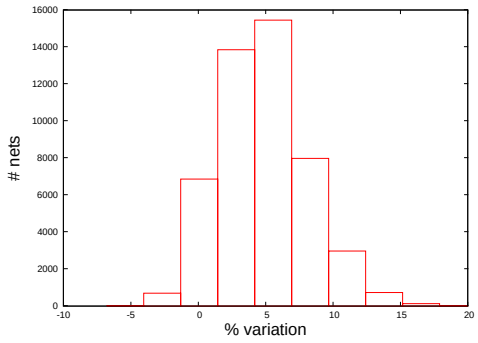

Fig. 13. Impact of etching and trapezoidal cross-sections on total cap for all nets (design *des*)

Figures 13 and 14 present the distribution of the *Total cap* variations for all nets and timing critical nets respectively of the design *des*. We evaluate from Table XIII that etching effects and the presence of trapezoidal conductor cross-sections increase the total net capacitances of timing critical nets by 10% on the average.

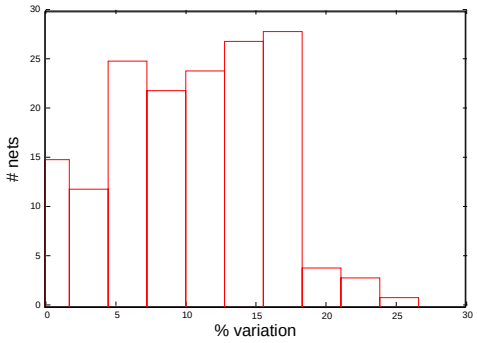

Fig. 14. Accurate impact of etching and trapezoidal conductor on total cap for timing critical nets (design *des*)

IV. CONCLUSION

In this paper, we presented the impact of modern process technologies on the electrical parameters of interconnects.

We conclude that fills can contribute significantly to the total capacitance of a net. In addition, we observe that varying fill patterns cause significantly varying impact on a net's total capacitance. It is thus important that fills be added carefully.

Results obtained on our set of designs indicate negligible impact of post CMP topography on interconnect parasitics, as compared to those computed with planar topography. This may be due to the fact that with inserted dummy fills, the post CMP topography is nearly planar, and hence can be ignored during parasitic extraction. However for larger designs in future technologies post CMP topograhies could be more non planar and may have larger impact on interconnect parasitic values.

We observe that the commonly found thin-dielectrics can be averaged out by using just one single ILD per metal layer. This introdcuces negligible errors (less than 1.5% in our designs) and substantially speeds up the capacitance extraction process.

Finally, we conclude that the impact of etching effects and trapezoidal conductor cross-sections can be significant on the total capacitance of a net. If the conductor side walls are nearly vertical then conductors can be approximated with rectangular cross-section to speed up the parasitic extraction process.

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