Curriculum Vitae

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Education

April 2000	Ph.D. degree from the University of Rochester. Research focus is on on-chip inductance in high speed integrated circuits.
May. 1998	Masters degree, University of Rochester, Department of Electrical and Computer Engineering. GPA is 4.0. Focus is on VLSI circuit design.
May 1996	Masters degree in Electronics, Cairo University, Faculty of Engineering, Electronics and Communications Department. Masters thesis: "Design of Stray-Insensitive Switched-Capacitor Filters." Percentile grade: 94.2%, Total grade: Distinction with Honors.
June 1993	Bachelor of Engineering, Cairo University, Faculty of Engineering, Department of Electronics and Communications. Percentile grade: 93.6 %, Total grade: Distinction with Honors.

Positions, Training, and Experience

July 2000 - Present	Associate Professor, Department of Electrical and Computer Engineering, Northwestern University.
July 1997 – Oct. 1999,	IBM Microelectronics, East Fishkill, NY. Position as a CAD development engineer. Gained experience in IBM EDA design tools. Developed research on the interaction between CMOS gates (0.25 and 0.18 μm IBM CMOS technology) and interconnect including on-chip inductance effects.

Patent Disclosures

1. Y. I. Ismail, E. G. Friedman, and J. L. Neves "Driving Inductive Interconnect Using Cascaded Buffers" IBM Microelectronics, August, 1999.
2. Y. Ismail and E. G. Friedman, "Model for Simulating Tree Structured VLSI Interconnect," United States Patent, No. 6,460,165, October 1, 2002.
3. Y. I. Ismail, "Efficient Model Order Reduction Via Multipoint Moment Matching", Northwestern University, Unites States Patent, No. 6,789,237, September 7, 2004.
4. Y. I. Ismail, C. Amin, M. H. Chowdhury, and C. V. Kashyap" Realizable Reduction of RLC Circuits Using Node Elimination," Semiconductor Research Corporation (SRC), (patent pending).
5. M. Ghoneima, M. Khellah, J. Tschanz, Y. Ye, Y. Ismail, V. De, "Achieving Low MCF by Tapering Segment Width In Opposite directions for Adjacent Bus Lines," US Patent Pending, Intel Corporation, 2003.

Publications

Books

1. Y. I. Ismail and E. G. Friedman "On-Chip Inductance in High Speed Integrated Circuits", Kluwer Academic Publishers, 2001.
2. Y. I. Ismail, Designing Large Global Nets, Chapter nine of the Edited Book: Chuck Alpert, Dinesh Mehta, and Sachin Sapatnekar, "Handbook on Algorithms for VLSI Physical Design", CRC press, 2006.

Refereed Journal Publications

1. J. Ku, S. Ozdemir, G. Memik, and Y. Ismail, "Thermal Management of On-Chip Caches through Power Density Minimization," IEEE Transactions on Very Large Scale Integration (VLSI) Systems. (accepted for publication)
2. J. Ku and Y. Ismail, "On Scaling of Temperature-Dependent Effects," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. (accepted for publication)

3. M. Khellah, M. Ghoneima, J. Tscahnz, Y. Ye, N. Kurd, J. Barkatullah, Y. Ismail and V. De, “A Skewed Repeater Bus Architecture for On-Chip Energy Reduction in Microprocessors,” IEEE Transactions on Circuits and Systems 1 : Fundamental Theory and Applications. (accepted for publication)
4. M. Ghoneima, M. Khellah, J. Tschanz, Y. Ye, Y. Ismail, and V. De, “Reducing the Effective Coupling Capacitance in Buses Using Threshold Voltage Adjustment Techniques,” IEEE Transactions on Circuits and Systems 1: Fundamental Theory and Applications, vol. 52, no. 9, pp. 1928-1933, September 2006.
5. M. Chowdhury and Y. Ismail, “Realistic Scalability of Noise in Dynamic Circuits,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 14, no. 6, June 2006, pp. 637-641.
6. M. Ghoneima, Y. Ismail, M. Khellah, J. Tschanz, V. De, "Formal Derivation of Optimal Active Shielding for Low-Power On-Chip Buses", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 25, no. 25, May 2006, pp. 821-836.
7. M. Ghoneima and Y. Ismail, “Optimum positioning of interleaved repeaters in bidirectional buses,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.24, no.3, March 2005. p. 461-469.
8. C. S. Amin, F. Dartu, and Y. I. Ismail, “Weibull based analytical waveform model,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 24, No. 8, pages 1156-1168, August 2005.
9. M. H. Chowdhury, C. Amin, Y. I. Ismail, " Realizable reduction of Interconnect Circuits Including Self and Mutual Inductances," IEEE Transactions on Computer-Aided Design, Vol. 24, No. 2, pp. 271-277, February 2005.
10. M. Ghoneima and Y. Ismail, “Utilizing the Effect of Relative Delay on Energy Dissipation in Low-Power On-Chip Buses,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 12, No.12, pages 1348-1359, December 2004.
11. Y. I. Ismail and C. Amin, “Computation of Signal Threshold Crossing Times Directly from Higher Order Moments”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 23, no. 8, pp. 1264-1276, August 2004.
12. S. Mei and Y. I. Ismail, “Modeling skin and proximity effects with reduced realizable RL circuits,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 12, No. 4, pp. 437-447, April 2004.
13. Y. I. Ismail, "Improved Model Order Reduction by Using Spacial Information in Moments," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 11, No. 5, pp. 900-908, October 2003.
14. Y. I. Ismail, "Effects of Inductance on the Propagation Delay and Repeater Insertion in VLSI Circuits: Summary," IEEE Circuits and Systems Magazine, April 2003. (invited paper).
15. S. Mei, C. Amin, and Y. I. Ismail, "Efficient Model Order Reduction Including Skin Effect," IEEE Canadian Journal of Electrical and Computer Engineering, Vol. 27, No.4, pages 189-194, October 2002. (invited paper).
16. Y. I. Ismail, "Cons and Pros of On-Chip Inductance," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 10, No. 6, pp. 685-694, December 2002.
17. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Inductance Effects in RLC Trees," To appear in the IEEE Journal of Circuits, Systems, and Computers, Vol. 11, No. 3, pp. 305-321, August 2002.
18. Y. I. Ismail and E. G. Friedman "On the Extraction of On-Chip Inductance," IEEE Journal of Circuits, Systems, and Computers JCSC, Vol. 12, No. 1, pp. 31-40, February 2003.
19. Y. I. Ismail and E. G. Friedman, “DTT: Direct Truncation of the Transfer Function-An Alternative For Moment Matching For Tree Structured Interconnect,” IEEE Transactions on Computer-Aided Design, Vol. 21, No. 2, pp. 131-144, February 2002.
20. Y. Massoud and Y. I. Ismail, "Grasping the impact of on-chip inductance", IEEE Circuits and Devices Magazine, Vol. 17, No. 4, pp. 14 – 21, July 2001. (invited paper).
21. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Exploiting On-Chip Inductance in High Speed Clock Distribution Networks," IEEE Transactions on Very Large Scale Integration (VLSI) Systems Vol. 9, No. 6, pp. 963 - 973, December 2001.
22. Y. I. Ismail, E. G. Friedman, and J. L. Neves, “Repeater Insertion in Tree Structured Inductive Interconnect,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 48, No. 5, pp. 471 – 481, May 2001.
23. Y. I. Ismail and E. G. Friedman, “Effects of Inductance on the Propagation Delay and Repeater Insertion in

VLSI Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 8, No. 2, pp. 195 – 206, April 2000. (IEEE CAS Outstanding Young Author Award).

24. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Equivalent Elmore Delay for *RLC* Trees," *IEEE Transactions on Computer-Aided Design*, Vol. 19, No. 1, pp. 83-97, January 2000.
25. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Figures of Merit to Characterize the Importance of On-Chip Inductance," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 7, No. 4, pp. 442 – 449, December 1999.
26. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Dynamic and Short-Circuit Power of CMOS Gates Driving Lossless Transmission Lines," *IEEE Transactions on Circuits and Systems 1: Fundamental Theory and Applications*, Vol. CAS-46, No. 8, pp. 950 - 961, August 1999.

Submitted Journal Papers

1. A. Shebaita and Y. Ismail, "Variable Threshold Voltage Design Scheme for CMOS Tapered Buffers," submitted to IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.
2. A. Shebaita, D. Das, H. Zhou, Y. Ismail, "Nostra-XTalk : A Predictive Framework for Accurate Static Timing Analysis in UDSM VLSI Circuits," submitted to IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.
3. D. Sinha, D. Khalil, H. Zhou, Y. Ismail, "A Timing Dependent Power Estimation Framework Considering Coupling," submitted to IEEE Transactions on Very Large Scale Integration (VLSI) Systems.
4. D. Khalil and Y. Ismail, "Optimum Sizing of Power Grids for IR Drop," submitted to IEEE Transactions on Circuits and Systems I.
5. J. Ku and Y. Ismail, "Thermal-Aware Methodology for Repeater Insertion in Low-Power VLSI Circuits," submitted to IEEE Transactions on Very Large Scale Integration (VLSI) Systems.
6. J. Ku and Y. Ismail, "Area Optimization for Leakage Reduction and Thermal Stability in Nanometer Scale Technologies," submitted to IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.
7. M. Ghoneima and Y. Ismail, "Accurate Decoupling of Capacitively Coupled Buses", submitted to *Transactions on Computer-Aided Design*.
8. C. S. Amin, Y. I. Ismail, F. Dartu, and N. Menezes, "Piece-wise Approximations of RLCK Circuit Responses using Moment Matching", submitted to *Transactions on Computer-Aided Design*.
9. C. S. Amin, F. Dartu, and Y. I. Ismail, "Modeling Unbuffered Latches for Timing Analysis", submitted *Transactions on Computer-Aided Design*.
10. M. Ghoneima, M. Khellah, J. Tschanz, Y. Ismail and V. De, "Serial Link Bus: A Low Power On-Chip Bus Architecture," submitted to T-CAS-I.
11. Shizhong Mei and Yehea I. Ismail, "Stable Parallelizable Model Order Reduction for Circuits with Frequency Dependent Elements", submitted to *IEEE Transactions on Computer-Aided Design*.
12. Shizhong Mei, Jamil Kawa, Charles Chiang, Yehea Ismail, "An Accurate Low Iteration Algorithm for Effective Capacitance Computation", submitted to *IEEE Transactions on Computer-Aided Design.*
13. M. H. Chowdhury, Y. I. Ismail, C. V. Kashyap, and B. L. Krauter, "Performance Analysis of Deep Sub micron VLSI Circuits in the Presence of Self and Mutual Inductance," *IEEE Transactions on Circuits and Systems 1: Fundamental Theory and Applications*
14. Y. I. Ismail, "Evaluating Noise Pulses in RLC Networks," IEEE Transactions on Very Large Scale Integration (VLSI) Systems. (in publication)
15. N. Hassan and Y. I. Ismail, "Maximizing Bit Rate on Wide Busses," IEEE Transactions on Very Large Scale Integration (VLSI) Systems. (in publication)
16. Masud H. Chowdhury, Yehea I. Ismail, "*Behavior and Analysis of Deep Sub-micron Integrated Circuits Including Self and Mutual Inductances, "* Submitted to IEEE Transaction on Circuits and Systems I (TCAS I).
17. M. Ghoneima and Y. Ismail, "Coupling Based Encoding for Low-Power On-Chip Buses," *IEEE Transactions on Circuits and Systems 1: Fundamental Theory and Applications*.

Refereed Conference Publications

27. A. Shebaita and Y. Ismail, "Variable Threshold Voltage Design Scheme for CMOS Tapered Buffers", Proceedings of the IEEE International Symposium on Circuits and Systems, May 2007.
28. J. Ku and Y. Ismail, "Attaining Thermal Integrity in Nanometer Chips", Proceedings of the IEEE International Symposium on Circuits and Systems, May 2007 (Invited paper).

29. J. Ku and Y. Ismail, "A Compact and Accurate Temperature-Dependent Model for CMOS Circuit Delay", Proceedings of the IEEE International Symposium on Circuits and Systems, May 2007.
30. D. Khalil and Y. Ismail, "Approximate Frequency Response Models for RLC Power Grids", Proceedings of the IEEE International Symposium on Circuits and Systems, May 2007.
31. K. Meng, F. Huebbers, R. Joseph, and Y. Ismail, "Modeling and Characterizing Power Variability in Multicore Architecture", Proceeding of the IEEE International Symposium on Performance Analysis of Systems and Software, April 2007.
32. A. Shebaita, D. Das, Y. Ismail, H. Zhou, and K. Killpak, "Nostra-XTalk: A Predictive Framework for Accurate Static Timing Analysis in UDSM VLSI Circuits," Proceedings of GLSVLSI, March 2007.
33. A.Shebaita, D. Petranovic and Y. Ismail, "Importance of Volume Discretization of Single and Coupled Interconnects," Proceedings of ICCAD, November 2006.
34. D. Sinha, D. Khalil, H. Zhou, Y. Ismail, "A Timing Dependent Power Estimation Framework Considering Coupling," Proceedings of ICCAD, pp. 401-407, November 2006.
35. D. Das, A. Shebaita, H. Zhou, K. Killpak, and Y. Ismail, "FA-STAC: A Framework for Fast and Accurate Static Timing Analysis with Coupling," Proceedings of ICCD, October 2006.
36. K. Meng, F. Huebbers, R. Joseph, and Y. Ismail, "Physical Resouce Matching under Power Asymmetry", P=ac2 Conference, IBM T.J. Watson Research Center, October 2006.
37. F. Huebbers, A. Dasdan, and Y. Ismail, "Computation of Accurate Interconnect Process Parameter Values for Performance Corners under Process Variations," Proceedings of DAC, pp. 797-800, June 2006.
38. M. Ghoneima, Y. Ismail, M. Khellah, and V. De, "Reducing the Data Switching Activity of Serialized Datastreams," Proceedings of ISCAS, pp. 1015-1018, May 2006.
39. D. Khalil and Y. Ismail, "Optimum Sizing of Power Grids for IR Drop," Proceedings of ISCAS, pp. 481-484, May 2006.
40. J. Ku, S. Ozdemir, G. Memik, Y. Ismail, "Power Density Minimization for Highly-Associative Caches in Embedded Processors," Proceedings of GLSVLSI, pp. 100-104, Apr-May 2006.
41. M. Ghoneima, M. Khellah, J. Tschanz, Y. Ismail, and V. De, "Reducing the Data Switching Activity on Serial Link Buses," Proceedings of ISQED, pp. 425-432, March 2006.
42. J. Ku and Y. Ismail, "Area Optimization for Leakage Reduction and Thermal Stability," Proceedings of ASP-DAC, pp. 231-236, January 2006. (invited paper)
43. M. Ghoneima, M. Khellah, J. Tschanz, Y. Ismail and V. De, "Serial Link Bus: A Low Power On-Chip Bus Architecture," Proceedings of ICCAD, pp. 541-546, November 2005.
44. A. Shebaita, C. Amin, F. Dartu, Y. Ismail, "Expanding the Frequency Range of AWE via Time Shifting", Proceedings of ICCAD, pp. 935-938, November 2005.
45. J. Ku, S. Ozdemir, G. Memik, Y. Ismail, "Thermal Management of On-Chip Caches Through Power Density Minimization", Proceedings of the IEEE/ACM International Symposium on Microarchitecture, pp. 283-298, November 2005.
46. M. Khellah, M. Ghoneima, J. Tschanz, Y. Ye, N. Kurd, J. Barkatullah, Y. Ismail and V. De, "A Skewed Repeater Bus Architecture for On-Chip Energy Reduction in Microprocessors," Proceedings of the 2005 IEEE International Conference on Computer Design, pp. 253-257, October 2005.
47. M. Ghoneima, E. Atoofian, A. Baniasadi and Y. Ismail, "Low Power Prediction Based Data Transfer Architecture," Proceedings of the 2005 IEEE CICC, pp. 313-316, September 2005.
48. J. Ku, M. Ghoneima and Y. Ismail, "The Importance of Including Thermal Effects in Estimating the Effectiveness of Power Reduction Techniques," Proceedings of the 2005 IEEE CICC, pp. 301-302, September 2005.
49. G. Memik, M. Chowdhury, A. Mallik, Y. Ismail, "Engineering Over-Clocking: Reliability-Performance Trade-Offs for High-Performance Register Files", Proceedings of IEEE/ACM International Conference on Dependable Systems and Networks (DSN), pp. 770-779, June - July 2005.
50. C. S. Amin, Y. I. Ismail, and F. Dartu, "Piece-wise Approximations of RLCK Circuit Responses using Moment Matching", DAC, pp.927-932, June 2005.
51. C. S. Amin, Y. I. Ismail, F. Dartu, and N. Menezes, "Statistical Timing, How Simple Can it Get? ", DAC, pp. 652-657, June 2005.
52. M. Ghoneima, M. Khellah, J. Tscahnz, Y. Ismail and V. De, "Skewing Adjacent Line Repeaters to Reduce the Delay and Energy Dissipation of On-Chip Buses," Proceedings of the 2005 IEEE International Symposium on Circuits and Systems, pp. 592-595, May 2005.
53. M. Ghoneima and Y. Ismail, "Accurate Decoupling of Coupled On-Chip Buses," Proceedings of the 2005 IEEE International Symposium on Circuits and Systems, pp. 4146-4149, May 2005.
54. C. S. Amin, Y. I. Ismail, F. Dartu, and N. Menezes, "Simplified Statistical Timing ", in TAU 2005.
55. N. Hassan, M. Ghoneima, and Y. I. Ismail, "Physical Limitations of On-Chip Interconnect," Great Lakes Symposium on VLSI, pp. 13-19, April 2005.
56. Y. I. Ismail and C. S. Amin, "Computation of Signal Threshold Crossing Times Directly from Higher Order Moments," ICCAD, pp. 246-253, November 2004.

57. C. S. Amin, F. Dartu, and Y. I. Ismail, "Modeling Unbuffered Latches for Timing Analysis", ICCAD, pp. 254-260, November 2004.
58. M. Ghoneima and Y. Ismail, "Formal Derivation of Optimal Active Shielding for Low-Power On-Chip Buses", Accepted in ICCAD, pp. 800-807, November 2004.
59. Masud H. Chowdhury, Yehea I. Ismail, **"***Analysis of Noise and its Scalability in Dynamic Circuits***,"** Custom Integrated Circuits Conference, pp. 505-508, October, 2004.
60. M. Ghoneima and Y. Ismail, "Low-Power On-Chip Bus Architecture Using Dynamic Relative Delays," Proceedings of SOCC, pp. 233-236, September 2004.
61. M. Ghoneima and Y. Ismail, "Utilizing the Effect of Relative Delay on Energy Dissipation in Low-Power On-Chip Buses," pp.66-69, ISLPED, August 2004.
62. M. Ghoneima and Y. Ismail, 'Effect Of Relative Delay On The Dissipated Energy In Coupled Interconnects', ISCAS, pp. II-525-8 Vol.2, May 2004.
63. M. Ghoneima and Y. Ismail , 'Low Power Coupling-Based Encoding For On-Chip Buses', pp. II-325-8 Vol.2, ISCAS, May 2004.
64. D. Dai, W. Wang, and Y. Ismail ,'Powder-Based Fabrication Techniques Of Single-Wall Carbon Nanotube Circuits', pp. III-701-4 Vol.3, ISCAS, May 2004.
65. Masud H. Chowdhury, Yehea I. Ismail, **"***Realistic Scalability of Noise in Dynamic Circuits***,"** International Workshop on System-On-Chip for Real Time Application, Canada, July 2004.
66. Masud H. Chowdhury, Yehea I. Ismail, **"**Possible noise failure modes in static and dynamic circuits**,"** International Workshop on System-On-Chip for Real Time Application, pp. 123-126, July 2004.
67. Shizhong Mei, Jamil Kawa, Charles Chiang, Yehea Ismail, "An Accurate Low Iteration Algorithm for Effective Capacitance Computation", International Workshop on System-On-Chip for Real Time Application, pp. 99-104, July 2004.
68. Chirayu S. Amin, Florentin Dartu, Yehea I. Ismail, "Weibull Based Analytical Waveform Model," Proc. of ICCAD, pp. 161-168, November 2003.
69. Chirayu S. Amin, Masud H. Chowdhury, and Yehea I. Ismail, "Realizable RLCK Circuit Crunching," Proc. of DAC, pp. 226-231, June 2003.
70. Shizhong Mei, Chirayu Amin, and Yehea I. Ismail, "Efficient Model Order Reduction Including Skin Effect," Proc. of DAC, pp. 232-237, June 2003.
71. Maged Ghoneima and Yehea Ismail,"Optimum positioning of interleaved repeaters in bidirectional buses," Proceedings of DAC, pp. 586 -591, June 2003.
72. Masud H. Chowdhury, Chirayu S. Amin, Yehea I. Ismail, Chandramouli V. Kashyap, and Byron L. Krauter, "Realizable Reduction of RLC Circuits Using Node Elimination," Proc. of ISCAS 2003, Vol III, pp. 494-497.
73. Shizhong Mei and Yehea Ismail, Modeling skin effect with reduced decoupled R-L circuits, International Symposium on Circuits and Systems 2003, Thailand, pages 588-591.
74. Masud H. Chowdhury and Yehea I. Ismail, **"***Analysis of Coupling Noise in Dynamic Circuits***,"** Proceedings of IEEE International Workshop on System on Chip (IWSOC), pp. 320-325, 2003.
75. *Noha Mahmoud, Yehea Ismail,* "Accurate Rise Time And Overshoot Estimation In RLC Interconnects" International Symposium on Circuits and Systems, pp. V-477-80 vol.5, 2003, Thailand.
76. M. H. Chowdhury, C. Amin, Y. I. Ismail, C. V. Kashyap, and B. L. Krauter, "Realizable Reduction of RLC Circuits," *Proceedings of the IEEE International Symposium on Circuits and Systems,* vol. 3, pp. III-494-97, May 2003. (invited paper)
77. Y. I. Ismail, "Efficient Model Order Reduction via Multi-point Moment Matching," in the proceedings of the IEEE/ACM International Conference on Computer Aided Design (ICCAD), pp. 767-774, November 2002.
78. Y. I. Ismail, "Evaluating Noise Pulses in RLC Networks," Proceedings of the 2002 IEEE International Symposium on Circuits and Systems, V-653-6 vol.5, 2002.
79. M. H. Chowdhury, Y. I. Ismail, C. V. Kashyap, and B. L. Krauter, "Performance Analysis of Deep Sub micron VLSI Circuits in the Presence of Self and Mutual Inductance," Proceedings of the 2002 IEEE International Symposium on Circuits and Systems, pp. 197-200, 2002.
80. S. Mei and Y. I. Ismail, "Efficient Model Order Reduction Including Skin Effect," International Workshop on SoC, pp. 189-192, July 2002. (invited paper)

81. M. H. Masud, S. Hsien, and Y. I. Ismail, "Circuit and Physical Level Challenges in SoC Circuits", IEEE World Multi-Conference on Systemics, Cybernetics and Informatics, 2001. (Best paper award).
82. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Exploiting On-Chip Inductance in High Speed Clock Distribution Networks," *IEEE Workshop on Signal Processing Systems*, pp. 642-652, October 2000.
83. Y. I. Ismail and E. G. Friedman, "Fast and Accurate Simulation of Tree Structured Interconnect", *IEEE Midwest Symposium on Circuits and Systems*, pp. 1130-4 vol.3, August 2000.
84. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Exploiting On-Chip Inductance in High Speed Clock Distribution Networks," IEEE Workshop on SiGNAL PROCESSING SYSTEMS. SiPS 2000. Design and Implementation, pp. 643-652, October 2000.
85. Y. I. Ismail and E. G. Friedman "Sensitivity of Interconnect Delay to On-Chip Inductance," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 403-407, May 2000.
86. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Repeater Insertion in Tree Structured Inductive Interconnect," *Proceedings of the ACM/IEEE International Conference on Computer-Aided Design*, pp. 420-424, November 1999.
87. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Optimizing *RLC* Tree Delays by Employing Repeater Insertion," *Proceedings of the IEEE ASIC Conference*, pp. 14-18, September 1999.
88. Y. I. Ismail, E. G. Friedman, and Jose L. Neves, "Equivalent Elmore Delay for *RLC* Trees," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 715-720, June 1999.
89. Y. I. Ismail and E. G. Friedman, "Effects of Inductance on the Propagation Delay and Repeater Insertion in VLSI Circuits," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 721-724, June 1999.
90. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Signal Waveform Characterization in *RLC* Trees," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 190-193, May 1999.
91. Y. I. Ismail and E. G. Friedman, "Repeater Insertion in *RLC* Lines for Minimum Propagation Delay," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 404-407, May 1999.
92. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Inductance Effects in *RLC* Trees," *Proceedings of the IEEE Great Lakes Symposium on VLSI*, pp. 56-59, March 1999.
93. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Transient Power in CMOS Gates Driving *LC* Transmission Lines," *Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems*, pp. 377-383, September 1998.
94. Y. I. Ismail and E. G. Friedman, "Optimum Repeater Insertion Based on a CMOS Delay Model for On-Chip *RLC* Interconnect," *Proceedings of the IEEE ASIC Conference*, pp. 369-373, September 1998.
95. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Power dissipated by CMOS Gates Driving Lossless Transmission Lines," *Proceedings of the IEEE International Symposium on Low-Power Electronics and Design*, pp. 139-141, August 1998.
96. Y. I. Ismail, E. G. Friedman, and Jose L. Neves, "Figures of Merit to Characterize the Importance of On-Chip Inductance," *Proceedings of the IEEE/ACM Design Automation Conference*, pp. 560-565, June 1998.
97. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Performance Criteria for Evaluating the Importance of On-Chip Inductance," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 244-247, May 1998.
98. Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Dynamic and Short-Circuit Power of CMOS Gates Driving Lossless Transmission Lines," *Proceedings of the IEEE Great Lakes Symposium on VLSI*, pp. 39-44, February 1998.

Activities, Honors, and Memberships

- Best Paper Award (see reference 81).
- 2002 Circuits and Systems Society Outstanding Young Author (see reference 23).
- 2002 NSF CAREER Award.
- 2002-2003 Best Teacher Award, ECE department, Northwestern University.

- On the Editorial Board of the *IEEE Transactions on Circuits and Systems 1: Fundamental Theory and Applications*, 2000-2004.
- On the Editorial Board of the *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2000-2006.
- Associate Editor-in-Chief of the *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2007-Present.
- On the IEEE VLSI Technical Committee
- On the IEEE CAS Society awards subcommittee 2003-2004
- On the Awards committee of ICCAD 2004 and 2005.
- Chair of the Gate Timing and power Subcommittee in ICCAD 2005.
- Technical Chair of the International Workshop on System on a Chip 2003, 2004.
- Technical Chair of the Great Lakes Symposium on VLSI Circuits 2005.
- General Chair of the Great Lakes Symposium on VLSI Circuits 2006.
- Editorial board of the Journal of Circuits, Systems, and Computers 2006 – present.
- Chair elect of the IEEE VLSI Technical Committee 2006 – present.
- On the technical committees of ICCAD, DAC, ISCAS, and MWCAS.
- Advisor to the NSF on many panels.
- Several of our papers were nominated for best paper awards in ICCAD and DAC.

Synergistic Activities:

Yehea Ismail is the associate Editor-in-Chief in the IEEE Transactions on Very Large Scale Integration (VLSI) Systems. He was an associate editor of the IEEE Transactions on Very Large Scale Integration (VLSI) Systems and IEEE Transactions on Circuits and Systems I. Fundamental Theory and Applications, and guest editor for a special issue of the IEEE Transactions on Very Large Scale Integration (VLSI) Systems on "On-Chip Inductance in High Speed Integrated Circuits". He was the Technical Chair for the IEEE International Workshop on System on a Chip, 2003, and 2004, the technical chair of the GLSVLSI 2005, and General chair of GLSVLSI 2006. He chairs the gate timing and power subcommittee in ICCAD 2005. He also conducted many tutorials in ICCAD, DAC,ISCAS, GLSVLSI, ICECS, and MWSCAS. He is on the committees of ISCAS 2000-2005, ICCAD 2004, ICCAD2005, DAC 2005, MWSCAS 2004-2005, GLSVLSI 2003-2006. He also reviewed many papers for the IEEE Transactions on Circuits and Systems II and IEEE Transactions on Computer Aided Design, and the IEE Electronics letters. He has also reviewed several conference papers for ISCAS 98-2005, ICCAD 2000-2005, ASIC 98 and 99, and GLSCAS 98-2005. The investigator conducted a panel on mixed signal design in the 2000 Midwest Symposium, chaired sessions in ISCAS 2002-2005 and ICCAD 2004, DAC 2005, IWSOC 2002, and gave presentations in several conferences including ISCAS 98-2005 DAC 98-2005, ICCAD 99-2005, IWSOC 02, and GLSVLSI 98, 99.

Tutorials and Talks

1. "Design and Analysis of High-Speed Integrated Circuits Including On-Chip Inductance," IEEE/ACM International Conference on Computer Aided Design (ICCAD), November 2002.
2. "High Performance Design Techniques in Nanometer Integrated Circuits", *IEEE International Symposium on Circuits and Systems*, May 2003.
3. "New Phenomena in Integrated Circuits in the Multi GigaHz Era", ICM, December 2003.
4. Many invited talks at Intel Circuits Research Labs and Strategic CAD Labs for the last three years.
5. Many Talks at IBM Austin Research Lab and Watson Research Labs.
6. Many talks at Industry in companies such as LSI Logic, MultiGig, OEA, Synopsis, Motorola, and Analog Devices.
7. Numerous presentations and several panels in circuit and VLSI conferences.
8. Talks at several universities.

Grants

1. "Managing Signal Integrity in Global Distribution Networks," SRC, 80K, October 2000-October 2001
2. "Maximizing the Bit Rate of Wide Busses," Intel, Hardware grant, equivalent 20K. December 2001.

3. "High-Speed Interconnect Design," Intel, Hardware grant, equivalent 20K. April 2002.
4. "CAREER: Investigating Circuit and Physical Level Issues in High-Performance Deep Submicrometer Circuits", NSF, CAREER Award, 400K. October 2002-October 2007.
5. "Integrated Frequency Dependent Modeling and Extraction of Coupled Signal, Clock, and Power Lines", SRC, 150K. April 2003- April 2006.
6. "Exploring Possibilities for Carbon Nanotubes as circuits and Interconnects", NSF, 100K. June 2004-June 2005.
7. "Improving the Accuracy of Timing Verification Tools", Intel, 75K. Gift Starting from June 2003.
8. "Optimizing the Delay, Power Consumption, and Noise of On-Chip Busses", Intel, 120K. Gift Starting from April 2003, April 2004, April 2005.
9. Research Gift in the general research area of high frequency circuit design, MultiGIG, 65K. Gift received on October 2004.
10. Intel Fellowship for my student Maged Ghoneima, 45K worth. Gift received on September 2004.
11. "DTEL: Proof of concept chip for the digital telescope", Argonne National Labs, 104K, September 2006.
12. "Self-Adjusting Architectures for Improved Performance, Yield, and Reduced Design Time", NSF, 400K, with Gokhan Memik, July 2006.
13. "Interconnect Design for Many-Core and 3-D Chips", Intel, 120K, September 2006.

Graduate Students:

Graduated 4 Ph.D. students and 2 Masters. The Ph.D. students are Chirayu Amin, who joined Intel Strategic CAD Research Labs, Masud Chowdhury who joined UIC as an assistant professor, Shizhong Mei, who joined Micron dynamic RAM design group, and Maged Ghoneima who joined Nvidia design group. The Masters student, Daniel Dai, joined Intel FPGA design team, and Kian Haghdad who joined Waterloo for Ph.D.

Currently I have 7 Graduate Students (5 Ph.D. and 2 Masters). I expect to graduate 1 more Ph.D. in 2007 and 2 in 2008. The 2 Masters Students are expected to graduate in 2006.

Teaching

Consistently scored above 5 in CTEC scores with very positive comments from students (see http://aquavite.northwestern.edu/ctec/ctec-view.cgi?netid=yis335). I was also most frequently cited for the last 5 years by the students in an exit survey among the best professors they had. Received best teacher award from the ECE department in 2002-2003.

Teaching three core courses in the VLSI area: ECE 391 "VLSI Systems Design", ECE 392 "VLSI Project" (FPGA), and ECE 393 "Design and Analysis of High-Speed Deep Submicron Circuits".