

On-Chip Inductance in High-Speed Integrated Circuits

Call for Papers:

The appropriate interconnect model has changed several times over the past two decades due to aggressive technology scaling. New, more accurate interconnect models were introduced when parasitic effects that were negligible in earlier technologies, could no longer be ignored. Currently, RC models are used to analyze high resistance networks while capacitive models are used for less resistive interconnects. However, on-chip inductance is becoming increasingly important since integrated circuits now operate at frequencies where the inductive impedance of thick wide wires is comparable to the wire resistance and line lengths are long enough, relative to signal rise times.

Furthermore, this trend shows every indication of spreading beyond the handful of lines it now affects. Operating frequencies which have increased dramatically over the past decade, are expected to maintain the same rate of increase over the next decade approaching 10 GHz by the year 2012. The use of thick upper level metals, large die sizes, and low resistance copper interconnect -- already used in many commercial CMOS technologies, will likewise continue. Finally because large die sizes enable more system integration, the use of long thick wide wires, once largely devoted to global clock distribution networks, will spread to critical data buses and control lines.

This special issue calls for papers dealing with the design and analysis of integrated circuits including on-chip inductance. Specific topics of interest are:

1. Characterizing the importance of on-chip inductance in current and future technologies.
2. Model order reduction techniques with sufficient accuracy to handle the complicated signals that can arise in RLC circuits.
3. Effects of on-chip inductance on the performance of integrated circuits.
4. Inductive coupling effects in integrated circuits.
5. Ldi/dt noise.
6. Design methodologies including on-chip inductance.
7. On-chip inductance extraction for timing and noise analysis.

Please note that this special issue does not deal with on-chip inductors manufactured on purpose for RF circuits. This issue will consider the above topics in relation to parasitic interconnect inductance.

Submission Deadline: August 15, 2001

Target Publication Date: April 2002

All manuscripts will be subject to the standard TVLSI review process. Prospective authors should submit postscript or PDF versions of their papers electronically to the new TVLSI web site no later than July 31, 2001. Late submissions will not be accepted. The web site address is:

<http://tvlsi-ieee.manuscriptcentral.com>

Authors should state clearly that their papers are for the Special Issue on On -Chip Inductance in High Speed Integrated Circuits both on the front page of the manuscript and in the Note to Editor field of the web submission form.

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