

Northwestern University  
Department of Electrical Engineering and Computer Science

**ECE 510-2 - Seminar: Power and Reliability in Architecture**  
Fall 2005

**Course Description**

This is a new seminar course which will explore advanced topics in two broad areas that will have a significant influence in computer systems design over the next decade: power related issues (energy/temperature) and reliability. The main learning vehicles will be readings of classic and recent research papers on both topics, followed by in-class discussions and critiques. Students will be expected to participate in all in-class sessions and occasionally lead a discussion. In addition, students will be required to write short (less than a page) critical analyses of the research papers.

This course is geared to graduate students in computer engineering and systems (architecture, VLSI/CAD, embedded systems, operating systems, programming languages/compiler design). There is no formal list of prerequisites, but students are expected to have a basic understanding of computer architecture principles.

**Instructor**

Professor Russ Joseph  
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Office Hours: Tuesday and Thursday 3:30pm-5:00pm or by appointment

**Class Meetings**

Discussion: Tuesday and Thursday 2:00-3:20pm  
Discussion: Tuesday 3:00-3:50pm  
Location: Tech LG62

## Prerequisite

Undergraduate knowledge of computer architecture.

## Webpage

The course webpage is available via Blackboard at: <http://www.ece.northwestern.edu/~rjoseph/ece510-2>

## Required Textbook

None.

## Tentative List of Papers/Topics

### Modeling Power in Processors

- David Brooks, Vivek Tiwari, and Margaret Martonosi. "Wattch: A Framework for Architectural-Level Power Analysis and Optimizations," 27th International Symposium on Computer Architecture (ISCA), Vancouver, British Columbia, June 2000.
- Integrated analysis of power and performance for pipelined microprocessors Zyuban, V.; Brooks, D.; Viji Srinivasan; Gschwind, M.; Pradip Bose; Strenski, P.N.; Emma, P.G.; Computers, IEEE Transactions on Volume 53, Issue 8, Aug. 2004 Page(s):1004 - 1016

### Managing Dynamic Power

- Reducing power with dynamic critical path information Seng, J.S.; Tune, E.S.; Tullsen, D.M.; Microarchitecture, 2001. MICRO-34. Proceedings. 34th ACM/IEEE International Symposium on 1-5 Dec. 2001 Page(s):114 - 123
- Pipeline gating: speculation control for energy reduction Srilatha Manne, Artur Klauser, Dirk Grunwald April 1998 ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture, Volume 26 Issue 3
- Mitigating Amdahl's Law through EPI Throttling Murali Annavaram, Ed Grochowski, John Shen June 2005 Proceedings of the 32nd Annual International Symposium on Computer Architecture ISCA '05

### Managing Static Power

- Stefanos Kaxiras, Zhigang Hu, and Margaret Martonosi, "Cache Decay: Exploiting Generational Behaviour to Reduce Cache Leakage Power," the 28th International Symposium on Computer Architecture. June, 2001.

- N.S. Kim, T. Austin, D. Blaauw, T. Mudge, K. Flautner, J.S. Hu, M.J. Irwin, M. Kandemir, and V. Narayanan, "Leakage Current: Moore's Law Meets Static Power," *Computer*, vol. 36, no. 12, Dec. 2003.
- S. Dropsho, V. Kursun, D.H. Albonesi, S. Dwarkadas, and E.G. Friedman, "Managing Static Leakage Energy in Microprocessor Functional Units," the 35th International Symposium on Microarchitecture, pp. 321-332, November 2002.

### **Thermal Considerations**

- K. Skadron, M.R. Stan, W. Huang, S. Velusamy, K. Sankaranarayanan, and D. Tarjan, "Temperature-Aware Computer Systems: Opportunities and Challenges." *IEEE Micro*, 23(6), Nov-Dec. 2003

### **Dealing With Power Variations**

- E. Grochowski, D. Ayers, and V. Tiwari, "Microarchitectural Simulation and Control of di/dt-induced Power Supply Voltage," The International Symposium on High Performance Computer Architecture (HPCA), February 2002.
- R. Joseph, D. Brooks, and M. Martonosi, "Control Techniques to Eliminate Voltage Emergencies in High Performance Processors," The International Symposium on High Performance Computer Architecture (HPCA), February 2003.
- Exploiting Resonant Behavior to Reduce Inductive Noise Michael D. Powell, T. N. Vijaykumar March 2004 ACM SIGARCH Computer Architecture News , Proceedings of the 31st Annual International Symposium on Computer Architecture ISCA '04, Volume 32 Issue 2

### **Run-time Monitoring**

- Canturk Isci, Margaret Martonosi, "Run-time Power Monitoring and Estimation in High-Performance Processors: Methodology and Experiences," *MICRO-36*, Dec. 2003.
- Tao Li and Lizy John, "Run-time Modeling and Estimation of Operating System Power Consumption," *SIGMETRICS* 2003.
- Russ Joseph and Margaret Martonosi, "Run-time Power Estimation in High-Performance Microprocessors" The International Symposium on Low Power Electronics and Design (ISLPED), August 2001.

### **Multiple Clock Domains**

- Power and performance evaluation of globally asynchronous locally synchronous processors Anoop Iyer, Diana Marculescu, May 2002, ACM SIGARCH Computer Architecture News, Volume 30 Issue 2
- G. Semeraro, G. Magklis, R. Balasubramonian, D.H. Albonesi, S. Dwarkadas, and M.L. Scott, "Energy Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," 8th International Symposium on High-Performance Computer Architecture, Feb 2002 (ps).
- Q. Wu, P. Juang, M. Martonosi, and D.W. Clark, "Formal Online Methods for Voltage/Frequency Control in Multiple Clock Domain Microprocessors. ASPLOS 2004".

### **Circuit-Level Timing Speculation**

- Dan Ernst, Nam Sung Kim, Shidhartha Das, Sanjay Pant, Toan Pham, Rajeev Rao, Conrad Ziesler, David Blaauw, Todd Austin, Trevor Mudge, and Krisztin Flautner, Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation, in the 36th Annual International Symposium on Microarchitecture (MICRO-36), December 2003

### **Power Aware Chip Multiprocessors**

- Single-ISA Heterogeneous Multi-Core Architectures: The Potential for Processor Power Reduction, Rakesh Kumar, Keith Farkas, Norm P. Jouppi, Partha Ranganathan, Dean M. Tullsen, In 36th International Symposium on Microarchitecture, December, 2003.
- Heat-and-run: Leveraging SMT and CMP to manage power density through the operating system. Michael Powell, Mohamed Gomaa, and T. N. Vijaykumar In Proceedings of the 11th International Conference on architectural support for programming languages and operating systems (ASPLOS), pages 260-270, October 2004

### **Transient Fault Detection and Recovery in SMT/CMP**

- Transient-Fault Recovery for Chip Multiprocessors Mohamed Gomaa, Chad Scarbrough, T. N. Vijaykumar, and Irith Pomeranz In Proceedings of the 30th Annual International Symposium on Computer Architecture (ISCA), pages 98-109, June 2003. architecture" in 2003)
- Opportunistic Transient-Fault Detection Mohamed Gomaa and T. N. Vijaykumar In Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA), pages 172-183, June 2005.
- Transient-Fault Recovery via Simultaneous Multithreading T. N. Vijaykumar, Irith Pomeranz, and Karl Cheng In Proceedings of the 29th Annual International Symposium on Computer Architecture (ISCA), pages 87-98, May 2002.

## **Testability**

- Rescue: A Microarchitecture for Testability and Defect Tolerance Ethan Schuchman and T. N. Vijaykumar In Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA), pages 160-171, June 2005.

## **On-line Hard Error Detection and Tolerance**

- Fred A. Bower, Daniel J. Sorin, and Sule Ozev. “A Mechanism for Online Diagnosis of Hard Faults in Microprocessors.” To appear in 38th Annual International Symposium on Microarchitecture (MICRO), November 2005
- Fred A. Bower, Paul G. Shealy, Sule Ozev, and Daniel J. Sorin. “Tolerating Hard Faults in Microprocessor Array Structures.” International Conference on Dependable Systems and Networks (DSN), June 2004.
- Background Reading: A Fault Tolerant Approach to Microprocessor Design. Chris Weaver and Todd Austin. International Conference on Dependable Systems and Networks (DSN), July 2001.

## **Architectural Vulnerability**

- Shubhendu S. Mukherjee, Christopher Weaver, Joel Emer, Steven K. Reinhardt, and Todd Austin, A Systematic Methodology to Compute the Architectural Vulnerability Factors for a High-Performance Microprocessor, in the 36th Annual International Symposium on Microarchitecture (MICRO-36), December 2003.
- Nicholas J. Wang, Justin Quek, Todd M. Rafacz, and Sanjay J. Patel, Characterizing the Effects of Transient Faults on a High-Performance Processor Pipeline, Proceedings of the 2004 International Conference on Dependable Systems and Networks, Florence, Italy, June 2004

## **Lifetime Management**

- Exploiting Structural Duplication for Lifetime Reliability Enhancement, Jayanth Srinivasan, Sarita V. Adve, Pradip Bose, Jude A. Rivers, To appear in the Proceedings of the 32nd International Symposium on Computer Architecture (ISCA'05) June 2005.
- The Case for Lifetime Reliability-Aware Microprocessors, Jayanth Srinivasan, Sarita V. Adve, Pradip Bose, and Jude A. Rivers, Proceedings of 31st International Symposium on Computer Architecture (ISCA '04) June 2004.

## Reliability Under Shared Memory

- SafetyNet: Improving the Availability of Shared Memory Multiprocessors with Global Checkpoint/Recovery, Daniel J. Sorin, Milo M. K. Martin, Mark D. Hill, and David A. Wood, International Symposium on Computer Architecture (ISCA), May 2002.

## Nano And Emerging Technologies

- NanoFabrics: Spatial Computing Using Molecular Electronics (2001) Seth Copen Goldstein, Mihai Budiu Proceedings of the 28th International Symposium on Computer Architecture 2001

## Clumsy Processors

- A Case for Clumsy Packet Processors A. Mallik and G. Memik In Proc. of IEEE/ACM International Symposium on Microarchitecture (MICRO-37), Portland, OR, Dec. 2004

## Discussion and Reading Assignments

The primary learning vehicles in this course will be the reading of technical papers and participation in class discussions. Nominally, the instructor will assign readings a week in advance (typically two papers per class meeting). Students are expected to have read the papers carefully and constructed a critical analysis of each paper.

The critical analysis should clearly identify strengths/contributions of the paper as well as potential weaknesses and areas for further work. In addition, students are encouraged to compare and contrast the approach/findings with other relevant work. Each critical analysis should be emailed to the instructor (plain text or ps/pdf are preferable) by class time the day the paper is to be discussed.

**Everyone benefits from a lively discussion, so be prepared for in class discussion by doing your reading!**

Occasionally (about twice during the quarter), each student will lead discussion on a research paper. Students should be prepared to give a brief summary of the work (using visual aids, e.g. PowerPoint or the blackboard when appropriate). Choice of topics/papers is on a first come-first serve basis. If you see a paper/topic that interests you, ask the instructor if you can lead the corresponding discussion. Schedule early to improve your chances of getting your first pick.

## Participation and Attendance

The quality of this course depends heavily on preparation, attendance, and participation of all the students. To that end, a significant component of the grade for this class will be your perfor-

mance/participation in class discussions. If you are unable to attend a class meeting, please email the instructor before hand.

## **Exams**

There will be no exams in this class.

## **Grading**

Grades will be assigned according to the following distribution:

Participation	50%
Critical Analysis	25%
Leading Discussion	25%

Because the grading in this class is more subjective than most technical classes, the instructor will give frequent feedback, so that students can make suitable adjustments.