

EECS453: Project 1 - Introduction to MP Simulators

Assigned: Jan 22, 2007

Due: Feb 5, 2007

1 Overview

This quarter you will be working on a research project which relates to multiprocessor design and evaluation. Consequently, you will need to be proficient with using a multiprocessor simulator. This assignment is intended to be a gentle introduction to the world of MP simulators.

2 Getting Started

In this class, we will use the M5 simulator (<http://m5.eecs.umich.edu/>). To complete this first project you will need to download, build, and install M5. The simulator should be able to build out of the box on recent Linux based x86 systems. If you do not have access to such a machine, please contact the instructor as soon as possible. I have links to the simulator, benchmarks, and help info on the course webpage. Please take a look at this info before you begin.

3 Logistics

For this assignment, you will need to evaluate multithreaded applications on symmetric multiprocessor (SMP) machines. Specifically, you will need to use M5 to investigate cache miss rates, bus traffic, and execution time under different system configurations. You will be provided with a base cache/processor configuration and you will perform a set of experiments designed to test the effect of scalability and cache capacity. Pick two experiments out of the following:

- keep L1 cache capacity fixed at 32KB, block size fixed at 64B and vary number of processors (2, 4, 8)

- keep number of processors fixed at 4, block size fixed at 64B and vary L1 cache capacity (16KB, 32KB, 64KB)
- keep L1 cache capacity fixed at 32KB, number of processors fixed at 4 and vary L1 cache block size (32B, 64B, 128B)

You should use the default cache coherence protocol (MSI), L2, and memory configurations. Pick any two benchmarks of your choosing out of the splash2 suite (see supplementary docs for more info about how to select benchmarks/configs). You should submit a brief project report (one page) which explains your configuration and reports:

- Data L1 cache miss rate (in each experiment, use the avg over all processors)
- L2 bus traffic (transactions per processor)
- Total performance (execution cycles)

You should explain *how* varying the parameters impacts your results. Then offer your guess as to *why* you see the results you do.