Inversed Temperature Dependence Aware Clock Skew Scheduling for Sequential Circuits

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***Abstract* — We present an Inversed Temperature Dependence (ITD) aware clock skew scheduling framework. Specifically, we demonstrate how our framework can assist dual-V_{th} assignment in preventing timing violations arising due to ITD effect. We formulate the ITD aware synthesis problem and prove that it is NP-Hard. Then, we propose an algorithm for synergistic temperature aware clock skew scheduling and dual-V_{th} assignment. Experiments on ISCAS89 benchmarks reveal that several circuits synthesized by the traditional high-temperature corner based flow with a commercial tool exhibit timing violations in the low temperature range while all circuits generated using our methodology for the same timing constraints have guaranteed timing.**

With the shrinking of feature sizes and increasing integration density, leakage power consumption has become a major concern. Dual-Vth synthesis is one of the approaches for reducing leakage power. In a typical dual-Vth design flow, circuits are synthesized at the high-temperature corner, as it is generally assumed that cell delay depends positively on temperature. At newer technologies this assumption becomes invalid. Under nominal supply voltages, delay of high-Vth cells might decrease with rising temperature [1-4]. As a result, at low temperature levels, paths containing high-Vth cells might exhibit longer delay and violate the timing constraint. This phenomenon, known as the Inversed Temperature Dependence (ITD), poses threats for the corner based dual-Vth synthesis flow.

A plausible way to meet timing constraints in the presence of ITD is to add timing margins. Vth assignment can be done at high temperature under an overly constrained clock period. However, determining a robust yet not too pessimistic margin is challenging [3]. In this work, we instead view temperature as a dimension of timing optimization and temperature dependent timing slacks as manageable resources. We propose to perform ITD aware clock skew scheduling during dual-Vth assignment to ensure timing correctness. Clock skew scheduling is a well known technique. However, traditional approaches define a static distribution of slacks among combinational logic stages. After dual-Vth synthesis, different combinational logic stages will be composed of different types of cells. Thus, they can exhibit different delay-temperature dependencies due to ITD. Hence, the temperature dependent timing slacks can be utilized more effectively if they can flow across the registers according to the actual need of different combinational logic stages as temperature fluctuates.

Circuit designs that adapt their slack dynamically has been studied [5, 6]. In a particular implementation [5] adaptive skew buffers were used, which adjust their delays proportional to temperature and redistribute slacks within sequential circuits. However, it was assumed that the delays of the combinational logic blocks always increase with rising temperature and hence, the ITD effect is not addressed. Despite this limitation, the basic concept of adaptive skew buffers provides a useful starting point towards coupling temperature with clock skew generation in presence of ITD.

Motivated by this observation, we propose to perform synergistic ITD aware clock skew scheduling and dual-V_{th} assignment to dynamically redistribute timing slacks globally within a sequential circuit to guarantee timing correctness. Experimental results on various benchmarks confirm that our technique can ensure timing closure. While the corner based flow using a commercial dual-V_{th} design tool can generate circuits exhibiting timing violations in low temperature range, our flow produces circuits with guaranteed timing. In terms of leakage power, our flow is at least as good as the corner based flow in most of the cases. Moreover, compared to a margin based synthesis flow which can eliminate the timing violations in most cases, our flow is superior in terms of leakage power reduction. The leakage power saving can be as large as 44.28% and 14.60% on average in comparison to the margin based flow.

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