

EDUCATION

University of California – Los Angeles

Ph.D., Computer Science Department

August 2003

Advisor: Majid Sarrafzadeh

Thesis: Design Planning in High-level Synthesis for Programmable Systems

Northwestern University

M.S., Electrical and Computer Engineering Department

May 2000

Bogazici University, Istanbul, Turkey

B.S., Department of Electrical and Electronic Engineering

July 1998

EMPLOYMENT

Northwestern University

Assistant Professor, Dept. of Electrical Engineering and Computer Science

September 2003 – Present

Consultant for Global Supercomputing

September 2005 – Present

Fujitsu Laboratories of America, Inc., Sunnyvale, CA

Research Intern

June - August 2001

University of California – Los Angeles

Research Assistant

December 2000 – August 2003

Northwestern University

Research Assistant

September 1998-December 2000

AWARDS AND HONORS

1. Co-author of Best Paper Award Finalist article presented at the IEEE/ACM International Conference on Computer Aided Design (ICCAD) 2007
2. National Science Foundation CAREER Award (2006)
3. Searle Center for Teaching Excellence Junior Fellow (2006-2007)
4. Co-author and presenter of the Best Paper Award Nominee article presented at the IEEE/ACM Design Automation Conference (DAC) 2005
5. Co-author of the Best Paper Award Nominee article presented at the IEEE/ACM Design Automation Conference (DAC) 2001

PUBLICATIONS

Refereed Journal Publications

- J1. Song Liu, Seda Ogrenci Memik, Yu Zhang, Gokhan Memik, "An Approach for Adaptive DRAM Temperature and Power Management", under review, *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*
- J2. Jieyi Long, Ja-Chun Ku, Seda Ogrenci Memik, Yehea Ismail, "SACTA: A Self-Adjusting Clock Tree Architecture for Adapting to Thermal-Induced Delay Variation", under review, *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*
- J3. Marco Santambrogio, Vincenzo Rana, Seda Ogrenci Memik, Donatella Sciuto, Umut Acar, "Combining Reconfigurable HW techniques and SW Adaptive Computation for a Novel SoC Design Methodology", under review, *ACM Transactions on Reconfigurable Technology and Systems (TRETs)*
- J4. Min Ni, Seda Ogrenci Memik, "A Fast Heuristic Algorithm for Multi-Domain Clock Skew Scheduling", under review, *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*

- J5. Jieyi Long, Hai Zhou, Seda Ogrenci Memik, "EBOARST: An Efficient Edge-Based Obstacle-Avoiding Rectilinear Steiner Tree Construction Algorithm", accepted by *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, to appear
- J6. Seda Ogrenci Memik, Nikolaos Bellas, Somsubhra Mondal, "Pre-synthesis Area Estimation of Reconfigurable Streaming Accelerators", accepted by *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, to appear
- J7. Rajarshi Mukherjee, Song Liu, Seda Ogrenci Memik, Somsubhra Mondal, "A High-Level Clustering Algorithm Targeting Dual V_{dd} FPGAs", accepted by *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, to appear
- J8. Jieyi Long, Seda Ogrenci Memik, Gokhan Memik, Rajarshi Mukherjee, "Thermal Monitoring Mechanisms for Chip Multiprocessors", accepted by *ACM Transactions on Architecture and Code Optimization (TACO)*, to appear
- J9. Seda Ogrenci Memik, Rajarshi Mukherjee, Min Ni, Jieyi Long, "Optimizing Thermal Sensor Allocation for Microprocessors", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27(3), March 2008
- J10. Rajarshi Mukherjee, Seda Ogrenci Memik, "An Integrated Approach to Thermal Management in High-Level Synthesis", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 14, No. 1., November 2006
- J11. Eren Kursun, Rajarshi Mukherjee, Seda Ogrenci Memik, "Early Quality Assessment for Low Power Behavioral Synthesis", *Journal of Low Power Electronics (JOLPE)*, Vol. 1, No. 3, pp. 273—285, December 2005
- J12. Ankur Srivastava, Seda Ogrenci Memik, B. K. Choi, Majid Sarrafzadeh, "On Effective Slack Management in Post-Scheduling Phase", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 24, No. 4, April 2005.
- J13. Seda Ogrenci Memik, Ryan Kastner, Elaheh Bozorgzadeh, "A Scheduling Algorithm for Optimization and Planning in High-level Synthesis", Majid Sarrafzadeh, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 10, No. 1, January 2005.
- J14. Elaheh Bozorgzadeh, Seda Ogrenci Memik, Xiaojian. Yang, Majid Sarrafzadeh, "Routability-driven Packing: Metrics and Algorithms for Cluster-based FPGAs, *Journal of Circuits, Systems, and Computers (JCSC)*, Vol. 13, No. 1, February 2004
- J15. Seda Ogrenci Memik, Aggelos K. Katsaggelos, Majid Sarrafzadeh, "FPGA Implementation and Analysis of an Iterative Image Restoration Algorithm", *IEEE Transactions on Computers (TC)*, Vol. 52, No. 3, March 2003
- J16. Ryan Kastner, Adam Kaplan, Seda Ogrenci Memik, Elaheh Bozorgzadeh, "Instruction Generation for Hybrid Reconfigurable Systems", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 7, No. 4, October 2002
- J17. Abhishek Ranjan, Kiarash Bazargan, Seda Ogrenci, Majid Sarrafzadeh, "Fast Floorplanning for Effective Prediction and Construction", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 9, No. 2, April 2001

Refereed Conference/Workshop Publications

- C1. B. Leung, Y. Pan, C. Schroeder, S. Ogrenci Memik, G. Memik, and M. Hartmann, "Towards an "Early Neural Circuit Simulator": An FPGA Implementation of Processing In the Rat Whisker System", to appear at the *International Conference on Field-Programmable Logic and Applications (FPL)*, September 9-11, 2008, Heidelberg, Germany
- C2. S. Liu, S. Ogrenci Memik, Y. Zhang, G. Memik, "An Approach for Adaptive DRAM Temperature and Power Management", in Proc. *ACM International Conference on Supercomputing (ICS)*, June 7-12, 2008, Kos, Greece
- C3. J. Long, S. Ogrenci Memik, "Automated Design of Self-Adjusting Pipelines", in Proc. *IEEE/ACM Design Automation Conference (DAC)*, June 8-13, 2008, Anaheim, CA
- C4. M. Ni, S. Ogrenci Memik, "Leakage Power-Aware Clock Skew Scheduling: Converting Stolen Time into Leakage Power Reduction", in Proc. *IEEE/ACM Design Automation Conference (DAC)*, June 8-13 2008, Anaheim, CA
- C5. S. Liu, S. Ogrenci Memik, Y. Zhang, G. Memik, "A Power and Temperature Aware DRAM Architecture", in Proc. *IEEE/ACM Design Automation Conference (DAC)*, June 8-13 2008, Anaheim, CA
- C6. J. Long, H. Zhou, S. Ogrenci Memik, "An $O(n \log n)$ Edge-Based Algorithm for Obstacle-Avoiding Rectilinear Steiner Tree Construction", in Proc. *ACM International Symposium on Physical Design (ISPD)*, April 13-16, 2008, Portland, OR

- C7. M. Santambrogio, S. Ogreneci Memik, "Managing Reconfigurable Resources in Heterogeneous Cores using Portable Pre-Synthesized Templates", in Proc. *International Symposium on System-on-Chip*, November 19-21, 2007, Tampere, Finland
- C8. M. Ni, S. Ogreneci Memik, "Early Planning for Clock Skew Scheduling during Register Binding", in Proc. *IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, November 5-8, 2007, San Jose, CA
- C9. J. Long, J. Ku, S. Ogreneci Memik, Y. Ismail, "A Self-Adjusting Clock Tree Architecture to Cope with Temperature Variations", in Proc. *IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, November 5-8, 2007, San Jose, CA [**IEEE/ACM William J. McCalla ICCAD Best Paper Award Finalist**]
- C10. M. Santambrogio, V. Rana, S. Ogreneci Memik, U. Acar, D. Scuito, "A Novel SoC Design Methodology Combining Adaptive Software and Reconfigurable Hardware", in Proc. *IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, November 5-8, 2007, San Jose, CA
- C11. M. Ni, S. Ogreneci Memik, "Self-Heating-Aware Optimal Wire-Sizing Under Elmore Delay Model", in Proc. *Design, Automation and Test in Europe (DATE)*, 16-20 April, 2007, Nice, France
- C12. Marco Santambrogio, Vincenzo Rana, Seda Ogreneci Memik and Donatella Scuito, "Combining Hardware Reconfiguration and Adaptive Computation for a Novel SoC Design Methodology", in Proc. *IEEE International Conference on Field-Programmable Technology (FPT)*, December 13-15, Bangkok, Thailand
- C13. R. Mukherjee, S. Mondal, S. Ogreneci Memik, "Thermal Sensor Allocation and Placement for Reconfigurable Systems", in Proc. *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 5-9 2006, San Jose, CA
- C14. R. Mukherjee, S. Ogreneci Memik, "Physical Aware Frequency Selection for Dynamic Thermal Management in Multi-Core Systems", in Proc. *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 5-9 2006, San Jose, CA
- C15. M. Ni, S. Ogreneci Memik, "Thermal-Induced Leakage Power Optimization by Redundant Resource Allocation", in Proc. *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 5-9 2006, San Jose, CA
- C16. S. Ogreneci Memik, M. Santambrogio, G. Agosta, "Adaptive Metrics for System-Level Functional Partitioning", in Proc. *Forum on Specification and Design Languages (FDL)*, September 19-22 2006, Darmstadt, Germany
- C17. S. Mondal, S. Ogreneci Memik, N. Bellas, "Pre-Synthesis Area Estimation of Reconfigurable Streaming Accelerators", in Proc. *International Conference on Field Programmable Logic and Applications (FPL)*, August 28-30 2006, Madrid, Spain
- C18. R. Mukherjee, S. Ogreneci Memik, "Systematic Temperature Sensor Allocation and Placement for Microprocessors", in Proc. *IEEE/ACM Design Automation Conference (DAC)*, July 24-28, 2006, San Francisco, CA
- C19. R. Mukherjee, S. Mondal, S. Ogreneci Memik, "A Sensor Distribution Algorithm for FPGAs with Minimal Dynamic Reconfiguration Overhead", in Proc. *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, June 26-29, 2006, Las Vegas, NV
- C20. S. Mondal, R. Mukherjee, S. Ogreneci Memik, "Fine-Grain Thermal Profiling and Sensor Insertion for FPGAs", in Proc. *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 21-24 2006, Kos, Greece
- C21. S. Mondal, S. Ogreneci Memik, N. Bellas, "Pre-synthesis Queue Size Estimation of Streaming Data Flow Graphs (Poster Presentation, 2-page extended abstract in the proceedings), *IEEE Symposium on FPGAs for Custom Computing Machines (FCCM)*, April 24-26, 2006, Napa, CA
- C22. D. Nguyen, G. Memik, S. Ogreneci Memik, and A. Choudhary, "Real-Time Feature Extraction for High Speed Networks", in Proc. *International Conference on Field Programmable Logic and Applications (FPL)*, August 24-26 2005, Tampere, Finland
- C23. R. Mukherjee, S. Ogreneci Memik, G. Memik, "Peak Temperature Control and Leakage Reduction During Binding in High-Level Synthesis", in Proc. *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, August 8-10 2005, San Diego, CA
- C24. R. Mukherjee, S. Ogreneci Memik, G. Memik, "Temperature-aware Resource Allocation and Binding in High-Level Synthesis", in Proc. *IEEE/ACM Design Automation Conference (DAC)*, June 13-17 2005, Anaheim, CA [**Best Paper Award Nomination**]
- C25. S. Mondal, S. Ogreneci Memik, "A Low Power FPGA Routing Architecture", in Proc. *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 23-26 2005, Kobe, Japan.
- C26. S. Mondal, S. Ogreneci Memik, "Fine-Grain Leakage Optimization in SRAM based FPGAs", in Proc. *Great Lakes Symposium on VLSI (GLSVLSI)*, April 17-19, Chicago, IL.

- C27. R. Jafari, S. Oğrenci Memik, M. Sarrafzadeh, “Quick Reconfiguration in Clustered Micro-Sequencer”, International Parallel and Distributed Processing Symposium (IPDPS), in Proc. Reconfigurable Architectures Workshop (RAW), April 4-5 2005, Denver, CO
- C28. S. Mondal, S. Oğrenci Memik, D. Das, “Hierarchical LUT Structures for Leakage Power Reduction” *Poster Presentation, ACM International Symposium on Field Programmable Gate Arrays (FPGA)*, February 20-22 2005, Monterey, CA
- C29. S. Mondal, S. Oğrenci Memik, “Resource Sharing in Pipelined CDFG Synthesis”, in Proc. IEEE/ACM Asia-South Pacific Design Automation Conference (ASP-DAC), January 18-21, Shanghai, China
- C30. R. Mukherjee, S. Oğrenci Memik, “Evaluation of Dual Vdd Fabrics for Low Power FPGAs”, in Proc. IEEE/ACM Asia-South Pacific Design Automation Conference (ASP-DAC), January 18-21, Shanghai, China
- C31. R. Mukherjee, S. Oğrenci Memik, “Power-driven Design Partitioning”, in Proc. *International Conference on Field-Programmable Logic and Its Applications (FPL)*, August 30 –September 1 2004, Antwerp, Belgium
- C32. R. Mukherjee, S. Oğrenci Memik, “Power Management for FPGAs: Power-driven Design Partitioning” (*Poster Presentation, 2-page extended abstract included in the proceedings*), *IEEE Symposium on FPGAs for Custom Computing Machines (FCCM)*, April 2004, Napa, CA
- C33. A. Srivastava, S. Oğrenci Memik, B. K. Choi, M. Sarrafzadeh, “Achieving Design Closure through Delay Relaxation Parameter”, in Proc. *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2003, San Jose, CA
- C34. S. Oğrenci Memik, G. Memik, R. Jafari, E. Kursun, “Global Resource Sharing for Synthesis of Control Data Flow Graphs on FPGAs”, in Proc. *IEEE/ACM Design Automation Conference (DAC)*, June 2003, Anaheim, CA
- C35. S. Oğrenci Memik, F. Fallah, “Accelerated SAT-based Scheduling of Control/Data Flow Graphs”, in Proc. *International Conference on Computer Design (ICCD)*, September 2002, Freiburg, Germany
- C36. E. Kursun, A. Srivastava, S. Oğrenci Memik, M. Sarrafzadeh, “Early Evaluation Techniques for Low Power Binding”, in Proc. *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, August 2002, Monterey, CA
- C37. E. Bozorgzadeh, S. Oğrenci Memik, R. Kastner, M. Sarrafzadeh, “Pattern Selection: Customized Block Allocation for Domain-Specific Programmable Systems”, in Proc. *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, June 2002, Las Vegas, NV
- C38. S. Oğrenci Memik, F. Fallah, “Accelerated Boolean Satisfiability-Based Scheduling for High-Level Synthesis”, *IEEE/ACM International Workshop on Logic & Synthesis (IWLS)*, June 2002, New Orleans, LA.
- C39. G. Memik, S. Oğrenci Memik, W. H. Mangione-Smith, “Design and Analysis of a Layer Seven Network Processor Accelerator Using Reconfigurable Logic”, in Proc. *IEEE Symposium on FPGAs for Custom Computing Machines (FCCM)*, April 2002, Napa, CA.
- C40. E. Bozorgzadeh, R. Kastner, S. Oğrenci Memik and M. Sarrafzadeh, “Pattern Selection in Programmable Systems” (*poster presentation*), *ACM International Symposium on Field Programmable Gate Arrays (FPGA)*, February 2002, Monterey, CA.
- C41. S. Oğrenci Memik, E. Bozorgzadeh, R. Kastner, M. Sarrafzadeh, “A Super-Scheduler for Embedded Reconfigurable Systems”, in Proc. *IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, November 2001, San Jose, CA
- C42. R. Kastner, S. Oğrenci Memik, E. Bozorgzadeh, M. Sarrafzadeh, “Instruction Generation for Hybrid Reconfigurable Systems”, in Proc. *IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, November 2001, San Jose, CA
- C43. K. Bazargan, S. Oğrenci, M. Sarrafzadeh, “Integrating Scheduling and Physical Design into a Coherent Compilation Cycle for Reconfigurable Computing Architectures”, in Proc. *IEEE/ACM Design Automation Conference (DAC)*, June 2001, Las Vegas, NV [**Best Paper Award Nomination**]
- C44. S. Oğrenci Memik, E. Bozorgzadeh, R. Kastner, M. Sarrafzadeh, “SPS: A Strategically Programmable System”, *International Parallel and Distributed Processing Symposium (IPDPS), Reconfigurable Architectures Workshop (RAW)*, April 2001, San Francisco, CA
- C45. E. Bozorgzadeh, S. Oğrenci Memik, M. Sarrafzadeh, “RPack: Routability-Driven Packing for Cluster-Based FPGAs”, in Proc. *Asia-South Pacific Design Automation Conference (ASP-DAC)*, January 2001, Yokohama, Japan
- C46. S. Oğrenci, K. Bazargan, M. Sarrafzadeh, “Image Analysis and Partitioning for FPGA Mapping”, in Proc. *IEEE Workshop on Signal Processing Systems (SiPS)*, October 2000, Lafayette, LA
- C47. K. Bazargan, R. Kastner, S. Oğrenci, M. Sarrafzadeh, “A C to Hardware/Software Compiler”, (*Poster Presentation, 2-page extended abstract included in the proceedings*), *IEEE Symposium on FPGAs for Custom Computing Machines (FCCM)*, April 2000, Napa Valley, CA

- C48. S. Ogrenç, A. K. Katsaggelos, M. Sarrafzadeh, "FPGA Implementation and Analysis of Image Restoration" (*poster presentation*), *ACM International Symposium on Field Programmable Gate Arrays (FPGA)*, February 2000, Monterey, CA

Invited Papers

- I1. S. Ogrenç Memik, "Design Planning in Hardware Compilers", Special Session on Synthesis for Programmable Systems, IASTED Parallel and Distributed Computing and Systems (PDCS), November 2003, Marina Del Rey, CA
- I2. S. Ogrenç Memik, A. Srivastava, E. Kursun, M. Sarrafzadeh, "Algorithmic Aspects of Uncertainty Driven Scheduling", IEEE International Symposium on Circuits and Systems (ISCAS), May 2002, Scottsdale, AZ

Book Chapters

- B1. E. Bozorgzadeh, R. Kastner, S. Ogrenç Memik, M. Sarrafzadeh, "Strategically Programmable Systems", *The Computer Engineering Handbook*, CRC Press, December 2001
- B2. E. Bozorgzadeh, A. Kaplan, R. Kastner, S. Ogrenç Memik, M. Sarrafzadeh, "Optimization for Reconfigurable Systems Using Hierarchical Abstraction", J. Cong and J. R. Shinnerl (editors), *Multilevel Optimization and VLSICAD*, Kluwer Academic Publishers, Boston, 2002

GRANTS

Research Grants

1. "Thermal Monitoring Infrastructures for Multi-core Systems"; Semiconductor Research Corporation (SRC) Grant No. G00639; 09/2007 (non-expiring), \$40,000; single investigator
2. "Computational and Hardware Models of Active Sensing Behaviors"; NSF IIS-0613568; 09/2006 – 09/2009; \$350,000; with Mitra Hartmann (PI) and Gokhan Memik
3. "Self-Adjusting Architectures/Circuits for Improved Performance and Reduced Design Complexity"; NSF CCF-0541337; 04/2006 – 04/2009; \$450,000; with Gokhan Memik (PI), Russ Joseph, and Yehea Ismail
4. "CAREER: Thermal-Aware Synthesis of Embedded Processors"; NSF CNS-0546305 (NSF CAREER Award); 03/2006 – 02/2011; \$400,000; single investigator
5. "Collaborative Research: High-Performance Techniques, Design and Implementation of Software Infrastructure for Change Detection and Mining"; NSF IIS-0536994; 09/2005 – 09/2008; this is a collaborative work with Indiana University; Northwestern amount: \$514,450; with Alok Choudhary (PI), Aggelos Katsaggelos, Ying Wu, and Gokhan Memik
6. "Collaborative Research: Ultra-scalable system software and tools for data-intensive computing"; NSF CCF-0444405; 10/2004 – 09/2008; this is a collaborative work with Pennsylvania State University and DePaul University - Northwestern amount: \$259,521; with Alok Choudhary (PI) and Gokhan Memik
7. Alumnae of Northwestern Research Initiation Grant, \$3,000; single investigator.
8. Motorola Undergraduate Research Grant to support the research of undergraduate student Elaine Jen.
9. NSF Undergraduate Research Funding for Modeling Timing Variation under Process Variation during High-level Synthesis
10. Equipment donation from Xilinx Inc. (FPGA development boards and design software worth \$10,000)

Educational Grants

11. "Design and Prototyping Laboratory for Computer Engineering Curriculum"; Murphy Society; 09/2007-08/2008; \$25,000; Primary Instructor, with Yehea Ismail
12. "Proposal for Modern Circuits and Signals Laboratory Development"; Murphy Society; 11/2005 – 11/2006; \$45,000; with Lawrence J. Henschen (PI), Robert Dick, Yehea Ismail, Mary Phillips, Russ Joseph, Gokhan Memik, Alan Sahakian, and Chi-Haur Wu

PROFESSIONAL ACTIVITIES

Service

- Editorial Boards
 - IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Associate Editor, Jan. 2007-ongoing
- Organizing Committee
 - Local Arrangements Co-Chair for the Great Lakes Symposium on VLSI (GLSVLSI) 2005

- Technical Program Committees
 - ACM/SIGDA PhD Forum at DAC 2008
 - International Symposium on Field Programmable Logic and Its Applications (FPL) 2008
 - Great Lakes Symposium on VLSI (GLSVLSI) (2008)
 - Applied Reconfigurable Computing (ARC) Workshop (ARC) 2008
 - Southern Conference on Programmable Logic (SPL) 2008
 - *System Design Track Chair*; IEEE/ACM International Conference on Computer Aided Design (ICCAD) (2007)
 - International Symposium on Field Programmable Logic and Its Applications (FPL) 2007
 - Great Lakes Symposium on VLSI (GLSVLSI) (2007)
 - Applied Reconfigurable Computing (ARC) Workshop (ARC) 2007
 - *High-Level Synthesis Track Chair*; IEEE/ACM International Conference on Computer Aided Design (ICCAD) (2006)
 - Design, Automation and Test in Europe (DATE) (2006)
 - Great Lakes Symposium on VLSI (GLSVLSI) (2006)
 - International Symposium on Field Programmable Logic and Its Applications (FPL) 2006
 - IEEE/ACM International Conference on Computer Aided Design (ICCAD) (2005)
 - International Symposium on Field Programmable Logic and Its Applications (FPL) 2005
 - Great Lakes Symposium on VLSI (GLSVLSI) (2005)
 - IEEE/ACM International Conference on Computer Aided Design (ICCAD) (2004)
 - Great Lakes Symposium on VLSI (GLSVLSI) (2004)
- Chaired sessions at ICCAD 2006, 2007, and will chair a session in 2008.
- Served on three NSF Panels between 2003-present
- Reviewer for over 30 conferences and journals, i.e., every major conference and journal in CAD, Reconfigurable Computing, and VLSI.

Invited Talks

1. “Thermal-Aware Design”, Electrical and Computer Engineering Department, University of Wisconsin-Madison, February 29, 2008
2. “Thermal-Aware Synthesis”, Strategic CAD Labs, Intel Inc, November 20, 2005, Hillsboro, OR
3. “An Architecture Exploration and Synthesis Framework for Reconfigurable Fabrics”, Center for Embedded Hardware Systems Research, Motorola Inc., February 15, 2005, Schaumburg, IL.
4. “Overview of Embedded and Hybrid Systems Research”, Privacy and Security Technologies Lab, Motorola Inc., July 28, 2004, Schaumburg, IL
5. “CAD Tools and Architectures for Low Power FPGAs”, Xilinx Inc., February 20, 2004, San Jose, CA

ADVISING, TEACHING, AND UNIVERSITY SERVICE

Current Graduate Students

Min Ni, PhD, expected graduation: 2009 (proposal: May 2007)
 Jieyi Long, PhD, expected graduation: 2011 (proposal: June 2008)
 Song Liu, PhD, expected graduation: 2011
 Brian Leung, PhD, expected graduation: 2012
 Chih-Hung Wu, PhD, expected graduation: 2013

Alumni

- PhD
 - Somsubhra Mondal, June 2007. Thesis title: Architectural Optimizations and Synthesis Tools for Improved Energy Efficiency and Faster Design Closure for FPGAs. First position: NeoKast Inc.
 - Rajarshi Mukherjee, June 2006. Thesis title: Thermal-aware design and analysis techniques for integrated circuits and high-performance microprocessor systems. First position: Senior Staff Engineer, Synopsys Inc.

- Undergraduate projects supervised: Aditya Khargonekar, Rina Harrison, Nicolas Holthaus, Elaine Jen, Chih-Hung Wu

Defense Committees

- PhD defense committee
Somshubra Mondal (chair), Rajarshi Mukherjee (chair), Ruiming Chen, Zhenyu Gu, Ja Chun Ku, DiaaEldin Khalil, Nikos Liveris, Serkan Ozdemir, Ahmed Shebaita, Jia Wang, Joseph Zambreno, David Zaretsky
- MS committee
David Nguyen, Seunghoon Kim, Sanghamitra Roy

University/Department Committees

- Computer Engineering Undergraduate Curriculum Committee (2003-ongoing)
- Participated as a Curriculum Committee member in the 2005 ABET accreditation process of the Computer Engineering Degree Program, co-authored the ABET report to address the concerns stated after site visit by evaluators, the full accreditation has been received after review of this report
- Computer Engineering Undergraduate Curriculum Sub-Committee for revision of freshman introductory course EECS 203 Introduction to Computer Engineering (2007-2008 academic year)
- Computer Science Undergraduate Curriculum Committee (2006-2007 academic year)
- Undergraduate Recruiting Committee (2006-2007 and 2007-2008 academic years)

Other University/Department Service

- Freshman academic adviser (2004 – ongoing)
- Active participation in graduate student recruiting of the EECS department. Volunteered for a pre-screening of applicants in 2006-2007 and 2007-2008 academic years
- Organized an event (co-sponsored by FREECS and EECS) for female undergraduate students of McCormick to present MS degree program options offered at the EECS department (May 2008)
- Host at the Society of Women Engineering (SWE) sponsored McCormick Career Day for Girls at Northwestern, 2005, 2006, 2007, 2008
- Hosted engineering lab demonstrations for Girl Scouts visiting Northwestern University