Place & Route: Using Silicon Ensemble

Introduction

In a typical digital design flow, hardware description language is used to model a design and verify desired behavior. Once the desired functionality is verified, the HDL program is then taken to an optimization tool such as Synopsys. The output of Synopsys is a gate level description of the desired circuit. The next step is to take this gate-level description to a place-and-route tool that can convert it to a layout level representation. In this tutorial, you will be introduced to a place-and-route tool called *Silicon Ensemble®*. This tool is capable of importing Verilog files as input. Regardless of the choice of your HDL source file for Synopsys, you can generate the output from Synopsys in Verilog format using the Save As… command. For the purposes of this tutorial, it will be assumed that you have a Verilog file ready to be placed and routed.

1. Silicon Ensemble Setup

1.1 The first thing you must do is make sure that `SE` appears in the .software file in your home directory. The .software file can be edited using your text editor of choice or by using the following commands:

```
cd ~
pico .software
```

If you had to add `SE` to your .software file, you must logout and re-login.

1.2 Next, create a directory that you can use for this tutorial:

```
mkdir directory_name
```

1.3 The files needed to use the *isucells* standard cell library in Silicon Ensemble have been placed in a .tar file. Download this file to your newly created directory. While in the new directory, extract the files using the following command:

```
tar xvf se.tar
```

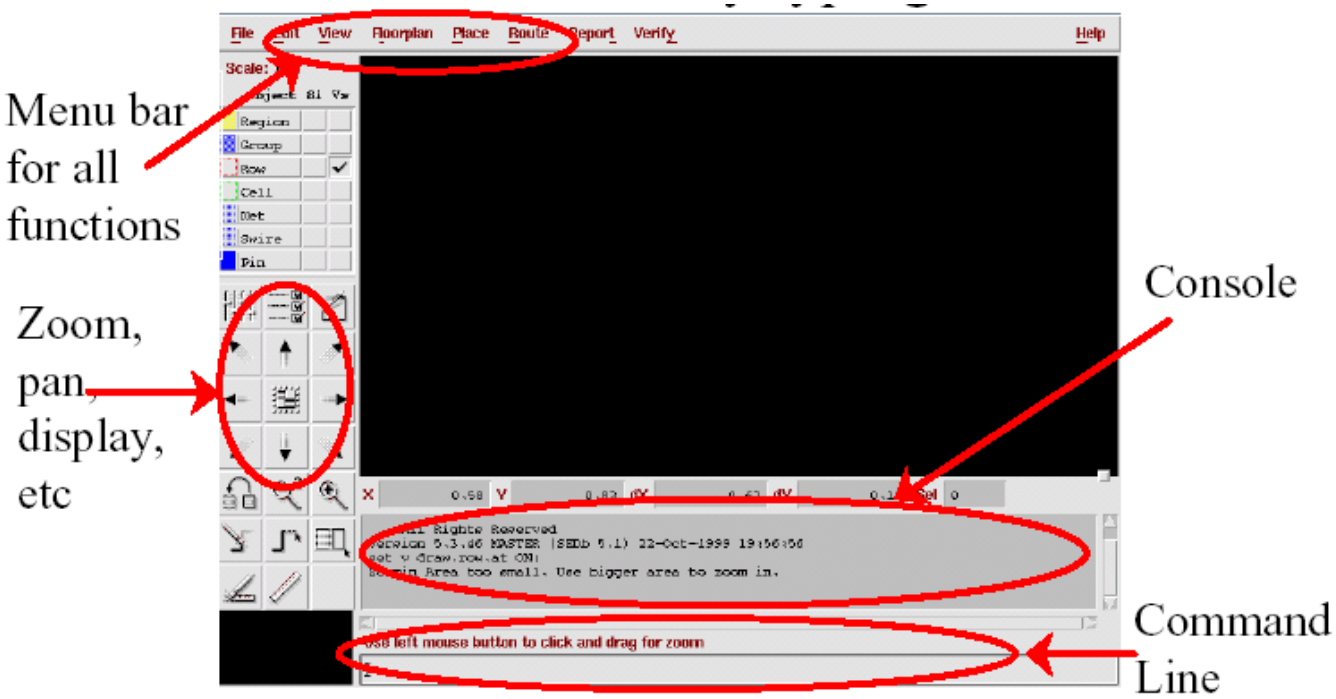
This will create four new directories. Change to the SE directory. This directory contains files needed by Silicon Ensemble and is the directory from which you will run Silicon Ensemble.

3. Starting and Importing files into Silicon Ensemble

3.1 To start Silicon Ensemble you need to type the following in your SE directory.

```
sedsm -m=60 &
```

3.2 Once Silicon Ensemble is up, acquaint yourself with the different menus at the top, the quick buttons on the lower-left, the select/view options in the upper-left, and the application output at the bottom of the window. The application output will give you feedback about what is going on similar to the CIW in Cadence.

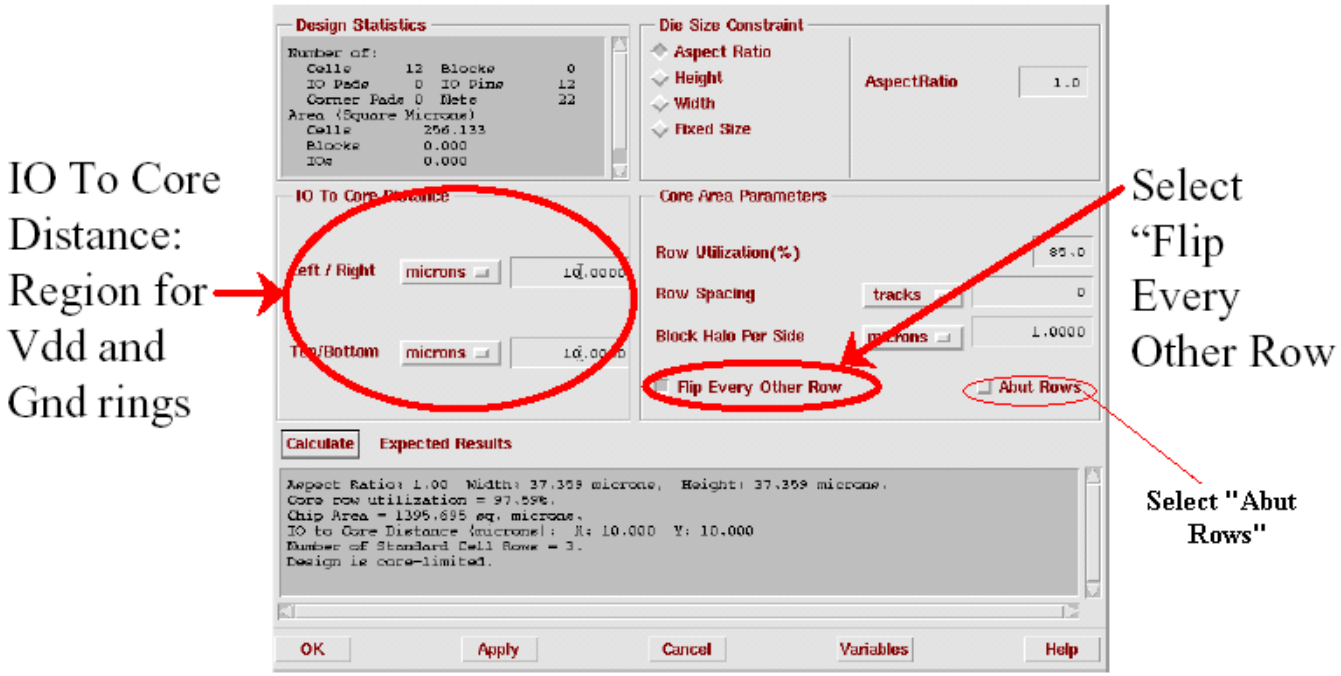


3.3 The first step is getting the reference library into Silicon Ensemble. To do this choose **File | Import → LEF…** The Import LEF window will pop up. Select the **LEF** of your Standard Cells. If you are using ISU standard cells then LEF file that you should use is **isucells.lef**. Click on the *case sensitive* and *clear existing design data* options at the bottom of the menu, and then click **OK**. There should be a bunch of output, but after it is complete there should be no errors or warnings. If there are, tell your TA. You now have the library information imported into Silicon Ensemble.

3.4 The next step is to get the design information into Silicon Ensemble. To do this, choose **File | Import → Verilog…** The Import Verilog window will pop up. Click on the **Browse…** button. Click on your verilog file then click **add.** Similarly, Now you have to import stubs.v file , which contains a module declaration of all standard cells. Click on **stubs.v** and click **add**. Click on the **OK** button. Type top module of your design for the *verilog top module* name. Click **OK**. Now every file that is needed for Silicon Ensemble to do Place and Route are given.

4. Initializing Floorplan / Placing IOs

4.1 After you are comfortable with the navigation arrows, initialize the floorplan by choosing **Floorplan | Initialize Floorplan …** An Initialize Floorplan window will pop up.

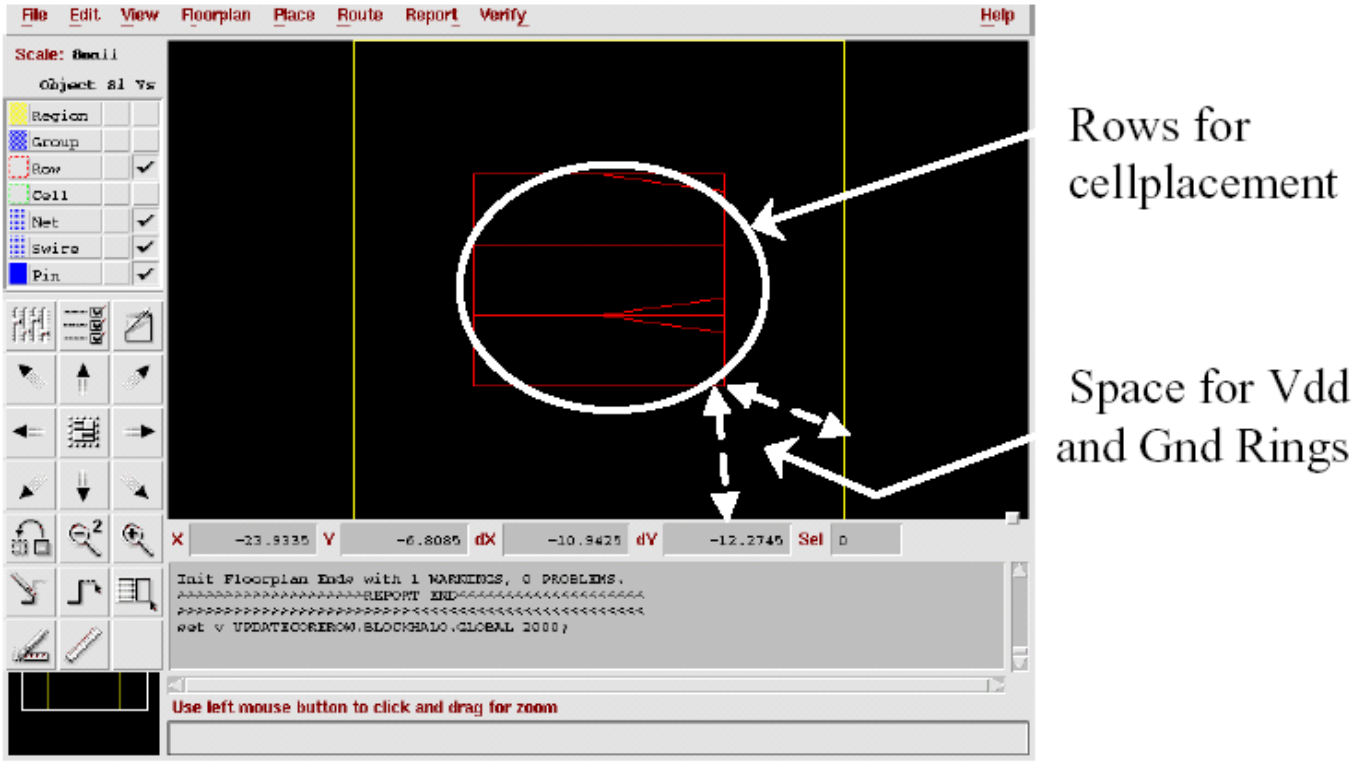


There are many fields in the window. To find the purposes of the various fields in the form, click on the **Help** button in the lower-right corner of the window. You will probably want to know the purpose of each field. When you use the tool on the final project, you will need to be able to set the variables correctly. Set the form so that the fields are as follows:

Left/Right	:	30 microns
Top/Bottom	:	30 microns

Also, make sure that the **Aspect Ratio** option is selected for the **Die Size Constraint** and that the **Aspect Ratio** is 1.0. The **Flip Every Other Row** and **Abut Rows** options should also be on. Now click the **Calculate** button. The bottom of the window will now contain some estimated layout statistics. Make sure that the expected core row utilization is less than 100%, by changing the ***Aspect Ratio*** in steps of +0.01 or – 0.01. Click **Calculate** to calculate core row utilization again. Click **OK**.

4.3 The standard cell rows should now be visible as red lines. You may need to go to **View | Redraw** to see this.



4.4 We now need to add rows, if there are any double-height cells(like D-Flip Flop) present in our design. In the main window, choose **Edit | Add → Row…** In the Add Row window, select dbl_core as the *Site Type*, and check the *Flip* and the *Abut Every Other Row* boxes.

Click on the **Area** button. Then, in the main window, click and drag an area that approximately covers all of the original row area. After you do this, the X-Y values should be filled in automatically. Click on the **OK** button.

4.5 Now that the floorplan is initialized, the I/O pins need to be placed. This is done by choosing **Place | IOs…** A Place IO window will open. For now, just choose the random option for the placement of the pins. Now you will see pins placed in your design.

5. Planning Power / Placing Cells / Compacting Floorplan

5.1 Now, the power routing scheme needs to be developed. To plan the power lines choose **Route | Plan Power …** A Plan Power toolbox will open. There should also be a yellow box enclosing the three rows in the middle. If you cannot see this, click the redraw icon. This is the path that the tool plans to route the power lines. You can change this by deleting/adding power paths.

5.2 To make the power paths click on the **Add Rings…** button. A PP Add Rings window will open. In the window fill in the form so that the following fields are set to the values given below:

Horizontal Layer:	Metal1
Vertical Layer:	Metal2
Core Ring Width (Horizontal):	4.8
Block Ring Width (Horizontal):	4.8
Core Ring Width (Vertical):	4.8
Block Ring Width (Vertical):	4.8
Core Ring Spacing:	Center (spacing will be grayed out)

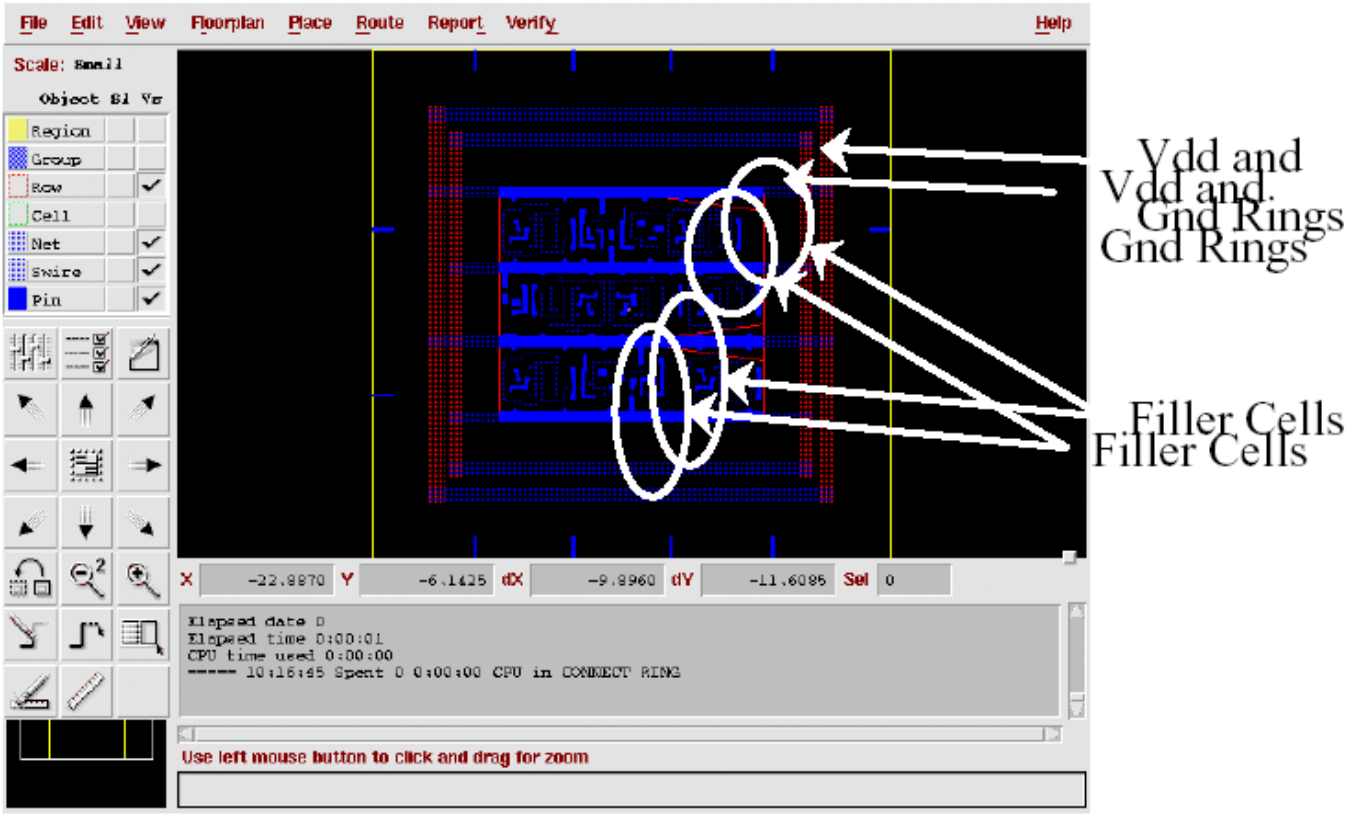
You should understand what each of the fields represents, because you will be using the tool for the final project. Again click on **Help** to learn about the commands and the fields/options associated with them. After, the values are entered click on **OK**. You should see a couple of blue and red rings encircle the rows. You are done planning the power, so click on **Close** in the Plan Power toolbox. After this step you will see Power Rings in two metal layers in Silicon Ensemble Window

5.3 After the power routing is planned, the cells need to be placed inside the rows. **Choose Place | Cells…** A Place Cells window will open. Click on **Help** to learn about the options that are available for the placement of cells. After you are done reading about the different options, close the Help window and click **OK** in the Place Cells window. If another box coming up that says use default template, click on **OK** in the window. You should be able to see the cells that are placed in the rows after this is done. If you are not able to see them make sure that they are visible in your Object Selection palette in the upper-left corner. In fact, you should probably make sure everything is visible. This will let you see everything that is happening in your design.

If placement fails, it is most likely because Silicon Ensemble cannot place the cells in the given area without overlaps. If this is the case, the information window at the bottom of the Silicon Ensemble window will give the following message: "Impossible to place without overlaps!" To solve this problem, you must start over by re-initializing the floorplan with relaxed constraints. The best constraint to change is the row utilization factor. By lowering this factor, you can increase the likelihood of placement without overlaps.

5.4 Next, we must add filler cells to the design. The purpose of filler cells is to maintain continuity in the rows by adding vdd! and gnd! lines and an n-well. The filler cells also contain substrate connections to improve substrate biasing.

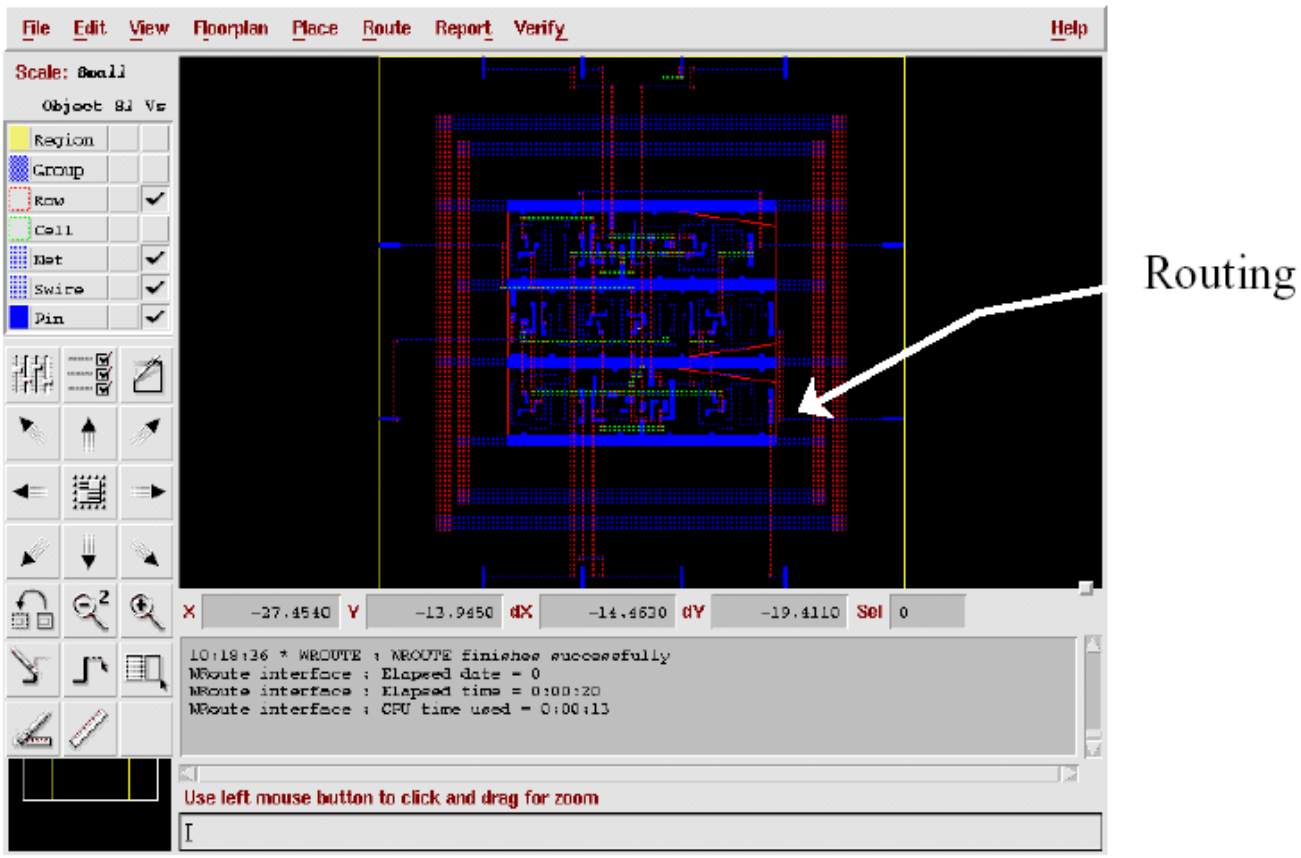
Choose **Place | Filler Cells → Add Cells…** Type `fill` in the *Model* and in the *Prefix* fields. In the first *Special Pin* and *Special Net* fields, type `vdd!` Likewise, in the second *Special Pin* and *Special Net* fields, type `gnd!` Click **OK**. Make sure that only 'North' and 'Flip South' boxes are checked, under Placement field. Design after Placing Pins, Power Rings , Cells and Filler Cells looks as shown in figure.



6. Routing the Design

6.1 To route *Power Rails*, choose **Route | Route Power → Follow Pins…** In the Sroute Follow Pins window, make sure vdd! and gnd! Are in the Nets field. Change the width field to 1.80. Click on **OK**. Now you can connect the vdd! and gnd! pins to the rings.

6.2 To route the cells together so that they are logically the same as the verilog description, choose **Route | Wroute.** Routing Mode window will open select Global and Final Route, then click ok. Now you will see in your Silicon Ensemble window, the routed design, you may need to zoom it to actually observe the routing. Design after routing looks as shown below,



6.3 Its time to check whether your design has been routed properly or not. To check the connectivity in your routed design with that of given verilog specification, choose Verify | Connectivity, a window will pop up, click OK. There should not be any errors.

7. Transferring the Design to Cadence

7.1 Now that the layout is complete, it is time to transfer it into Cadence. Go to **File | Export → GDS II…** In the Export GDSII window, specify your desired output file name in the *GDS-II File* field. Also, make sure that gds2.map appears in the *Map File* field. Click **OK**.

7.2 Before you import your design into cadence, its always better to create the library into which you want to import your design. Even if you don't create library, when you import your design the library will be created automatically, but it will give some problems. Create library and attach AMI06 library to it.

7.3 From the CIW window, choose **File | Import → Stream…** Type path of your GDS output file in the *Input File* field. Also, type *topcell* name in the *Top Cell Name* field. In the *Library Name* field, type the library name to which you are transferring the layout. Next, click the **Options** button. In the Stream In Options form, select the *Retain Reference Library (No Merge)* option, then click **OK**. Click **OK** in the stream in form to stream in the GDS file.

7.4 After a while, a message saying whether or not the stream-in was successful will appear (Ignore the warnings, if there is only one). If the stream-in was unsuccessful, see the PIPO.LOG file for more information. The layout should now be in the correct library in Cadence.

7.5 A few changes need to be made to the layout. First, open the layout to make sure all of the cells and routing are present. You may notice that there are no pins, just labels where the pins should be. To fix this, choose **Create | Pins From Labels…** Change the *Pin Layer* to respective pin layer (for example if it says metal1 then Pin Layer should be metal1 pin layer (metal1.pn)). Also, change both the *width* and *length* fields to 0.9. Click **OK**.

Now, we need to change all of the labels from the metal 1 layer to the text layer. This is necessary to avoid DRC errors about "Improperly formed shapes". The labels' layer can be changed by clicking on each (so it is highlighted), choosing **Edit | Properties…** , and changing the layer to text.dg.

Finally, we need to change the directions of the pins. When creating pins from labels, Cadence makes all of the pins "inputOutput" type. The pin directions can be changed by viewing the pin properties, clicking on *Connectivity* and changing *I/O Type* to the correct type for the pin.

8. Conclusion

This tutorial gave a brief overview of Silicon Ensemble. Many features of this powerful tool were not employed in this tutorial. You may want to explore some of these other features and options. For example, Silicon Ensemble is able to place and route according to timing specifications. You may want to explore some of these features, since they may significantly improve the final layout of your design.

Note: All figures are copied from following document,
www-mtl.mit.edu/research/icsystems/research/ pres/cheewe/cheewe_setutorial.pdf