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Research Interests

Effects of Technology Scaling on Processor Architectures
Processor Architectures for 3D Design
Low-Power Memory Architectures
Thermal Aware Design
VLSI Systems Design

Education

Ph.D. in Computer Eng., **Expected: June 2009** **09/2004 – present**	NORTHWESTERN UNIVERSITY, Evanston / IL Department of Electrical Engineering and Computer Science *Advisor: Prof. Gokhan Memik*
B.S. in Microelectronics, **09/2000 - 07/2004**	SABANCI UNIVERSITY, Istanbul / Turkey Faculty of Engineering and Natural Sciences Graduated with GPA: 3.89/4.00. Ranking: 5th/ 150
08/2000	Entrance into the university via the nationwide university entrance examination. Ranking: 3rd among 1,500,000 participants
Lower Education, **High School Diploma** **09/1997 – 06/2000**	ISTANBUL ATATURK HIGH SCHOOL OF SCIENCE, Istanbul / Turkey Graduated with GPA: 5.00/5.00. Ranking: 1st / 96

Dissertation Research

Title: *Mitigating the Effects of Process Variations through Microarchitectural Techniques*

My doctoral research centers around analyzing, modeling, and mitigating the effects of Process Variations (PV) on processor architectures in current and future manufacturing technologies. This research is motivated by the move towards smaller technology nodes, effectively pushing into the fundamental limits of CMOS processing and making it harder to precisely manufacture each device on chip. At the same time, higher levels of integration due to smaller geometries result in increased static power consumption and temperature. If not handled properly, these effects pose a serious threat to chip yield levels, power consumption, and reliability.

During my doctoral study, I evaluated different trade-offs available to computer architects between yield, performance, and power consumption on single and multi-core systems. I have also analyzed the economical implications of processor architecture designs and shown that a) there is a strong correlation between the architectural configuration of a processor and its price and b) it is possible to achieve significant increases in bottom-line revenue by utilizing microarchitectural techniques. Finally, I investigated how PV would effect 3D integration. I argue that if these effects are not considered, switching to 3D integration would cause a significant drop in yield levels. I proposed two different techniques, which not only offset the negative impact of PV but actually result in increased yield levels, improving the feasibility of 3D integration.

Publications

Refereed Journal Publications

[CAL 07]   Microarchitectures for Managing Chip Revenues under Process Variations
A. Das, S. Ozdemir, G. Memik, J. Zambreno, A. Choudhary
IEEE Computer Architecture Letters, Vol 6, June 2007.

[TVLSI 07]	Thermal Management of On-Chip Caches Through Power Density Minimization
	J. C. Ku, S. Ozdemir, G. Memik, Y. Ismail
	IEEE Transactions on Very Large Scale Integration Systems, Vol 15-5, May 2007.

Refereed Conference Publications

| ***Under Submission*** | Quantifying and Coping with Parametric Variations in 3D-Stacked Microarchitectures |
| | S. Ozdemir, P. Yan, A. Das, G. Memik, G. Loh, A. Choudhary |

[DAC 09]	Selective Wordline Voltage Boosting for Caches to Manage Yield under Process Variations
	Y. Pan, J. Kong, S. Ozdemir, G. Memik, S. W. Chung
	To appear in 46th DAC, San Francisco / CA, July 2009.

[MICRO 08]	Evaluating the Effects of Cache Redundancy on Profit
	A. Das, B. Ozisikyilmaz, S. Ozdemir, G. Memik, A. Choudhary
	MICRO-41, Lake Como / Italy, Nov. 2008.

[SC 07]	Variable Latency Caches for Nanoscale Processor ***Best Student Paper Award***
	S. Ozdemir, A. Mallik, J. C. Ku, G. Memik, Y. Ismail
	SC'07, Reno / NV, Nov. 2007.

[ICCD 07]	Evaluating Voltage Islands in CMPs under Process Variations
	A. Das, S. Ozdemir, G. Memik, A. Choudhary
	ICCD'07, Lake Tahoe / NV, Oct. 2007.

[ASGI 07]	Mitigating the Effects of Process Variations: Architectural Approaches for Improving Batch Performance
	A. Das, S. Ozdemir, G. Memik, J. Zambreno, A. Choudhary
	ASGI'07 (in conjunction with ISCA'07), San Diego / CA, June 2007.

[MICRO 06]	Yield-Aware Cache Architectures
	S. Ozdemir, D. Sinha, G. Memik, J. Adams, H. Zhou
	MICRO-39, Orlando / FL, Dec. 2006.

[GLSVLSI 06]	Power Density Minimization for Highly-Associative Caches in Embedded Processors
	J. C. Ku, S. Ozdemir, G. Memik, Y. Ismail
	GLSVLSI, Philadelphia / PA, Apr. 2006.

[MICRO 05]	Thermal Management of On-Chip Caches Through Power Density Minimization
	J. C. Ku, S. Ozdemir, G. Memik, Y. Ismail
	MICRO-38, Barcelona / Spain, Nov. 2005.

[MMS 05]	A Type-II 4th Order Fractional-N Frequency Synthesizer Design for Bluetooth Applications
	S. Yaldiz, S. Ozdemir, A. Ergintav, I. Tekin, A. Bozkurt, Y. Gurbuz
	Mediterranean Microwave Symposium (MMS'2005), Athens / Greece, Sep. 2005.

Technical Reports

T1.	Variable Latency Caches for Nanoscale Processor
	S. Ozdemir, J. C. Ku, A. Mallik, G. Memik, Y. Ismail
	NWU-EECS-06-16, Northwestern University, June 2006.

T2.	Thermal Management of On-Chip Caches Through Power Density Minimization
	J. C. Ku, S. Ozdemir, G. Memik, Y. Ismail
	CUCIS-2005-07-001, Center for Ultra-scale Computing and Information Security, July 2005.

Patents

P1.	Yehea Ismail, Gokhan Memik, Ja Chun Ku, Serkan Ozdemir
	Thermal Management of On-Chip Caches Through Power Density Minimization
	US Patent 20080120514 filed by Northwestern University.

Professional Experience

Reviewer	IEEE Transactions on Very Large Scale Integration (TVLSI)
	IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)
	IEEE/ACM International Symposium on Microarchitecture (MICRO)
External (Secondary) Reviewer	ACM Transactions on Architecture and Code Optimization (TACO)
	IEEE Transactions on Computers (TC)
	ACM Transactions on Design Automation of Electronic Systems (TODAES)
	IEEE/ACM International Symposium on Computer Architecture (ISCA)
	IEEE/ACM International Symposium on High-Performance Computer Architecture (HPCA)
	IEEE Dependable Systems and Networks (DSN)
	ACM Symposium on Applied Computing (SAC)
	IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI)
	IEEE International Symposium on Workload Characterization (IISWC)
	IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)
	Design Automation and Test in Europe (DATE)
Membership	IEEE Student Member since 2003

Work Experience

Research Assistant **09/2004 – present**	Northwestern University, Evanston / IL Department of Electrical Engineering and Computer Science Member of MRL – Microarchitecture Research Lab Advisor: Prof. Gokhan Memik
Research Intern **06/2006 – 09/2006**	IBM Austin Research Lab., Austin / TX Summertime Blues Innovation Challenge Project description: Design of a thermal characterization EDA tool for a unified platform for microprocessor high level modeling for performance, power and verification. Advisor: Dr. Emrah Acar and Dr. Jun Sawada
Undergraduate Research Intern **06/2003 – 09/2003**	ASELSAN, Ankara / Turkey Microelectronics, Guidance and Electro-Optics Division/Thermal Systems Design Department Project description: Design of a video deinterlacer card for thermal cameras using VHDL.

Teaching Experience

McCormick School of Engineering and Applied Science, Northwestern University

ASIC and FPGA Design	Junior level, Winter 2005
Engineering Analysis – I	Freshmen level, Fall 2005
Computer Architecture – I	Junior level, Winter 2006
Introduction to Parallel Computing	Junior level, Fall 2006
Computer Architecture – I	Junior level, Winter 2007
Advanced Digital Logic Design	Junior level, Spring 2007
Microprocessor System Design	Sophomore level, Spring 2007
Introduction to Parallel Computing	Junior level, Fall 2007
Computer Architecture – I	Junior level, Winter 2008
Computer Architecture – I	Junior level, Fall 2008
Computer Architecture Project	Junior level, Winter 2009

Faculty of Engineering and Natural Sciences, Sabanci University

Discrete Mathematics	Sophomore level, Spring 2003

Honors and Awards

2007	Best Student Paper Award at International Conference for High Performance Computing, Networking, Storage and Analysis (SC'07)
2004 - 2005	Walter P. Murphy Fellowship, Northwestern University
2000 - 2004	Merit Scholarship for academic excellence, Sabanci University, Istanbul, Turkey
2000	3rd ranking among 1.5 million high school graduates in the annual central nationwide university entrance exam (OSS 2000), Turkey
2000	Summa cum laude, Istanbul Ataturk High School of Science
1999	1st mention, the Scientific and Technical Research Council of Turkey (TUBITAK) Regional Olympiad in Informatics, Ankara, Turkey

Computer Skills

Programming Experience: Ansi-C, Visual C++, Java, Matlab, Intel x86 and MIPS Assembly, Parallel Programming with MPI and OpenMP, Perl, Tcl/Tk, HTML

Modeling and Hardware Description Languages: VHDL, Verilog

Architecture Simulation Tools: SimpleScalar, CACTI, HotSpot, Simics, GEMS

VLSI Tools: Cadence (Spectre, Virtuoso), Mentor Graphics (Modelsim), Synopsys (Design Compiler), Synplicity (Synplify PRO), Xilinx ISE, SPICE

Personal Information

Visa Status: F1

Country of Citizenship: Turkey

References

Available upon request.