YAN PAN

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Research Interests

Some of my main research interests are:

- Interconnection Network for Chip Multi-Processors **[ISCA'09, HPCA'10]**
  - Adopting nanophotonics for efficient on-chip communication and arbitration
  - Network topologies and adaptive designs
  - Network-on-Chip evaluation methodologies, evaluation framework.
- Architectural Techniques for Mitigating Process Variation **[DAC '09] [DAC '10]**
  - Process variation modeling/mitigation for cache/3D structures
- Empathic Computer Architectures: User- aware low-power techniques **[MICRO '08]**

Education

Ph.D. in Computer Engr., 09/2007 – present
NORTHWESTERN UNIVERSITY, Evanston / IL
Department of Electrical Engineering and Computer Science
Advisor: Prof. Gokhan Memik (GPA 4.0/4.0)

M.S. in Computer Engr., 08/2003 – 05/2006
NATIONAL UNIVERSITY OF SINGAPORE, Singapore
Electrical and Computer Engineering Department (GPA: 4.9/5.0)

B.S. in Elec. & Info. Engr. 09/1998 – 07/2002
SHANGHAI JIAOTONG UNIVERSITY, Shanghai, China
Electrical Engineering Department (GPA: 88/100)

Work Experience

Research Assistant 09/2007 – present
Northwestern University, Evanston / IL
Department of Electrical Engineering and Computer Science
Member of MRL – Micro-architecture Research Lab **Advisor: Prof. Gokhan Memik**

Engineer 08/2006 – 08/2007
Chartered Semiconductor Manufacturing, Singapore. (NASDAQ: CHRT)
New Technology Prototyping for 65nm Products, Yield Analysis / Enhancement

Engineer 08/2002 – 07/2003
Dracom Communication Co.,Ltd, Shanghai, China.
Embedded System Development, Proprietary Network Protocol Design

Teaching Experience

McCormick School of Engineering and Applied Science, Northwestern University, ***Teaching Assistant***

Engineering Analysis – I	Freshmen level, Fall 2008
C++ Programming	Sophomore level, Winter 2008
Microprocessor System Design	Junior Level, Fall 2009

Electrical and Computer Engineering Department, Faculty of Engineering, National University of Singapore, ***Teaching Assistant***

Microporcessors — Senior level, 2004 – 2006
Feedback Rating 4.7/5 (Department Faculty Avg. : 3.9/5)

Publications

[DAC'10] *Quantifying and Coping with Parametric Variations in 3D-Stacked Microarchitectures*
S. Ozdemir, Y. Pan, A. Das, G. Memik, G. Loh and A. Choudhary
To appear in Design Automation Conference (DAC), Anaheim, CA, June 2010
(acceptance rate: 148/607 = 24.4%)

[HPCA'10] *FlexiShare: Energy-Efficient Nanophotonic Crossbar Architecture through Channel Sharing*
Yan Pan, J. Kim and G. Memik
Int'l Symp. on High Performance Computer Architecture (HPCA), Bangalore, India, Jan. 2010
(acceptance rate: 32/175 = 18.3%)

[PICA'09] *Tuning Nanophotonic On-Chip Networks Designs for Improving Memory Traffic*
Yan Pan, J. Kim and G. Memik
Workshop on Photonic Interconnects & Computer Architecture (PICA)
(Held in conjunction with MICRO'42), New York, NY, Dec. 2009

[DAC'09] *Selective Wordline Voltage Boosting for Caches to Manage Yield under Process Variations*
Yan Pan, J. Kong, S. Ozdemir, G. Memik and S.W. Chung
Design Automation Conference (DAC), San Francisco, CA, Jul. 2009
(acceptance rate: 148/682 = 21.7%)

[NOCS'09] *Exploring Concentration and Channel Slicing in On-Chip Network Router*
P. Kumar, Yan Pan, J. Kim, G. Memik and A. Choudhary
Int'l Symp. on Networks-on-Chip (NOCS), San Diego, CA, May. 2009
(full paper acceptance rate: 23/126 = 18.3%)

[ISCA'09] *Firefly: Illuminating Network-on-chip with Nanophotonics*
Yan Pan, P. Kumar, J. Kim, G. Memik, Y. Zhang, A. Choudhary
Int'l Symp. on Computer Architecture (ISCA), Austin, TX, Jun. 2009
(acceptance rate: 43/210 = 20.5%)

[MICRO'08] *Power to the People: Leveraging Human Physiological Traits to Control Microprocessor Frequency*
A. Shye, Yan Pan, B. Scholbrock, J. S. Miller, G. Memik, P. Dinda, R. Dick
Int'l Symp. on Microarchitecture (MICRO), Lake Como, Italy, Nov. 2008.
(acceptance rate: 40/210 = 19.0%)
Nominated for Best Paper Award - Top 8 papers selected by program committee

[FPL'08] *Towards an 'Early Neural Circuit Simulator': A FPGA Implementation. of Processing in the Rat Whisker System*
B. Leung, Yan Pan, C. Schroeder, S. Memik, G. Memik, MJZ Hartmann
FPL'08, Heidelberg, Germany, Sept. 2008.
(full paper acceptance rate: 69/247 = 27.9%)

[TENCON'06] *Functional Unit Selection in Superscalar Microprocessors for Low Power*
Yan Pan, Teng Tiow Tay
TENCON '06, Hongkong, China, Nov. 2006.

[IFIPVLSI'05] *Time Domain Constraints on Switching with Gated-GND Cache Structures for Static Power Reduction*
Yan Pan, Teng Tiow Tay
IFIP VLSI-SOC '05, Perth, Australia, Oct. 2005.

[JSEKE'05] *HW/SW Co-Design for Low Power ALUs by Exploiting Slack in Instruction Interdependence*
Tengtiow Tay, Karsin Ng, Yan Pan
Int. Jrnl. of Software Engineering & Knowledge Engineering. Vol. 15, No. 2 (Aprl 2005)

Professional Experience

Reviewer
ACM Symposium on Applied Computing (SAC)
ACM Transactions on Architecture and Code Optimization (TACO)

ACM Transactions on Design Automation of Electronic Systems (TODAES)
Design Automation and Test in Europe (DATE)
IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI)
IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)
IEEE Transactions on Computer Aided Design (TCAD)
IEEE Transactions on Computers (TC)
IEEE Transactions on VLSI (TVLSI)
International Conference on Parallel Processing (ICPP)
International Symposium on High-Performance Computer Architecture (HPCA)

Membership IEEE Student Member
ACM SIGARCH Student Member

Selected Awards

Fall 2007 Walter P. Murphy Fellowship, Northwestern University

Sept. 2001 **First Prize in China**. National Undergraduate Electronic Design Contest
Project: Customizable Waveform Generator using Direct Digital Synthesis

1999-2001 First Prize of Excellence Scholarship (Top 5%)

Dec. 1999 Exceptional Student of Shanghai Jiao Tong University (Top 1%)

Computer Skills

Proficient Programming in: Ansi-C/C++ and Perl

Architecture Simulation Tools: SimpleScalar, M5, CACTI, HotSpot, Booksim, Simics, GEMS

Data Processing Tools: R-Tool, JMP, MS EXCEL, Matlab

VLSI Tools: HSPICE, Cadence (Spectre, Virtuoso), Mentor Graphics (Modelsim)

Familiar with Programming in: Visual C++/MFC, Intel x86 and ADSP Assembly, Javascript, HTML

Simulator Development

NoC Simulator: Architectural simulator based on BookSim
Modeling Firefly hybrid hierarchical on-chip network topology
Modeling integrated/external network concentration
Modeling FlexiShare architecture with Token-Stream arbitration

Process Variation Simulator: Automated HSPICE net-list generator for Cache Critical Path based on CACTI 5.1
Fine-grain device parameter mapping under process variation

Neural Circuit Simulator: Rat Whisker Neural Circuit Simulator
Modeling 1st stage spiking neuron with statistical firing
Modeling Summation based 2nd stage neurons

Personal Information

Visa Status: F1 **Country of Citizenship:** China, P.R.

References

Prof. Gokhan Memik. EECS Department, Northwestern University. Email: g-memik@northwestern.edu

Prof. John Kim. CS Department, KAIST. Email: jjk12@kaist.edu